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December 21, 2011

U.S. Nuclear Regulatory Commission
Document Control Desk
11555 Rockville Pike
Rockville, MD 20852

ATTENTION: To whom it may concern

SUBJECT: Rolls-Royce Response to Request for Additional Information Re: Rolls-Royce Civil Nuclear "***SPINLINE 3*** Digital Safety Instrumentation and Control Platform" Topical Report (TAC NO. ME3600)

REFERENCES: (1) Project Number 0773: ***SPINLINE 3*** Digital Safety Instrumentation and Control Platform (TAC No. ME3600)
(2) Letter, Jonathan G. Rowley (NRC) to Mark Burzynski (Rolls-Royce), "Request for Additional Information Re: Rolls-Royce Civil Nuclear "***SPINLINE 3*** Digital Safety Instrumentation and Control Platform" Topical Report (TAC NO. ME3600)", November 7, 2011

NRC provided a request for additional information regarding the review of the Rolls-Royce ***SPINLINE 3*** Digital Safety Instrumentation and Control Platform Topical Report. The Rolls-Royce response to this request for additional information is provided by an enclosure to this letter.

Rolls-Royce hereby submits the following documents in connection with the referenced NRC project.

Document Title	Rolls-Royce Document Number	Versions: Proprietary (P), Non-proprietary (NP)	Notes
Response To Request For Additional Information - ***SPINLINE 3*** Digital Safety Instrumentation and Control Platform - Project No. 773	N/A	P	New document
Response To Request For Additional Information - ***SPINLINE 3*** Digital Safety Instrumentation and Control Platform - Project No. 773	N/A	NP	New document
Attachment 1 Rolls-Royce Procedure, Project Development Process	8 303 314 L	P	New document

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Attachment 2 Rolls-Royce Procedure, System Design (Safety Systems)	8 303 334 F	P	New document
Attachment 3 Rolls-Royce Drawing	3 008 630 A (Sheet 6)	P	New document
Attachment 4 Power-One K Series with PFC Data Sheet, 150 – 280 Watt AC-DC Converters	N/A	NP	New document
Attachment 5 Power-One P Series Data Sheet, 90 - 194 Watt DC-DC Converters	N/A	NP	New document
Attachment 6 Microsens Ethernet Media Converter	N/A	NP	New document
Attachment 7 Modicon Ethernet Cabling System Quick Reference Guide, Ethernet Hub 10 Mbps 3TP/2FL	N/A	NP	New document
Attachment 8 Modicon Ethernet Cabling System Quick Reference Guide, Ethernet Hub 10 Mbps 4TP	N/A	NP	New document
Attachment 9 Phoenix Contact FL MC 10/100 BASE-T/FO G1300ST Converter	N/A	NP	New document

Rolls-Royce considers some of the material contained in the response to be proprietary and requests that the proprietary documents be withheld from public disclosure. In accordance with 10 CFR 2.390, "Public inspections, exemptions, requests for withholding", an affidavit is enclosed identifying the specific portions of the above documents that are proprietary and the basis for making that determination.

Proprietary and non-proprietary versions of the response to the request for additional information are provided. Nonproprietary version of Attachments 1 - 3 are not provided based on the guidance in NRC Information Notice (IN) 2009-07. As noted in IN 2009-07, in instances in which a nonproprietary version would be of no value to the public because of the extent of the proprietary information, the agency does not expect a nonproprietary version to be submitted.

All documents are submitted electronically.

If you have any questions related to this submittal, please contact me at 423-756-9730 extension 12 or by e-mail at mark.j.burzynski@ds-s.com.

Sincerely,

Mark J. Burzynski
US I&C Licensing Manager
Rolls-Royce

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Tel: (423) 756-9730
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Affidavit

STATE OF TENNESSEE)

)

COUNTY OF HAMILTON)

1. In accordance with 10 CFR 2.390, "Public inspections, exemptions, requests for withholding", Rolls-Royce requests withholding from public disclosure of the documents listed in Table 1, which is attached to this affidavit.
2. I am familiar with the criteria applied by Rolls-Royce to determine whether certain Rolls-Royce information is proprietary. I am familiar with the policies established by Rolls-Royce to ensure the proper application of these criteria.
3. As required by 10 CFR 2.390, Rolls-Royce has included in Table 1 the following information:
   - Identity of the document or part sought to be withheld;
   - Declaration of the basis for proposing the information be withheld, encompassing considerations set forth in § 2.390(a);
   - Specific statement of the harm that would result if the information sought to be withheld is disclosed to the public; and
   - Locations in the documents of all information sought to be withheld.
4. As required in § 2.390(b)(4); Rolls-Royce wishes to note that the request for withholding from public disclosure applies to pages that contain commercially sensitive information that Rolls-Royce normally discloses only under a Non-Disclosure Agreement (NDA). This commercially sensitive information is not available in public sources and is the type of information customarily held in confidence by Rolls-Royce and our competitors.

5. Rolls-Royce is transmitting this information to NRC in confidence.

6. As noted in Table 1, release of this information in a public forum could cause harm to Rolls-Royce by revealing trade secrets and/or commercially sensitive design and operational details and technical processes related to designing, building, and/or operating a ***SPINLINE 3*** digital safety instrumentation and control system.

7. As Rolls-Royce US I&C Licensing Manager, I have been specifically delegated responsibility for reviewing the information sought to be withheld, and I am authorized to apply for its withholding on behalf of Rolls-Royce.

8. The foregoing statements are true and correct to the best of my knowledge, information, and belief.

Mark J. Burzynski

Mark J. Burzynski
US I&C Licensing Manager
Rolls-Royce

Sworn to and subscribed before me
this 20th day of December, 2011

Jordan Maier

Notary Public

My commission expires: 5/9/2012

JORDAN MAIER
STATE OF TENNESSEE
NOTARY PUBLIC
HAMILTON COUNTY

Table 1. Documents requested for withholding from public disclosure

Document Title	Document Number	Part of document sought to be withheld from public disclosure	Basis for proposing the information be withheld, encompassing considerations set forth in § 2.390(a)	Specific statement of the harm that would result if the information sought to be withheld is disclosed to the public	Location(s) in the document of all information sought to be withheld (Notes 1 and 2)
Response To Request For Additional Information - ***SPINLINE 3*** Digital Safety Instrumentation and Control Platform - Project No. 773	N/A	Portions of response, as marked by brackets [[ ]].	Trade secrets and / or commercial information as per § 2.390(a)(4)	Rolls-Royce would be harmed by disclosure of aspects of the identified commercially sensitive information, which is of value to a competitor because it would enable them to make direct comparisons between the design features, equipment qualification processes, and commercial grade dedication methods for their ***SPINLINE 3*** safety I&C platform.	Some or all of the responses to questions 1, 2, 3, 4, 5, 6, 7, 8, 11, 13, 14, 17, 18, 20, 23, 26, and 28 as marked by brackets [[ ]]:
Attachment 1 Rolls-Royce Procedure, Project Development Process	8 303 314 L	Entire document (see Note 2).	Trade secrets and / or commercial information as per § 2.390(a)(4)	Rolls-Royce would be harmed by disclosure of aspects of its proprietary technical processes for safety systems design and hardware module development. These processes underpin the integrity of ***SPINLINE 3*** equipment, which is an important competitive advantage for Rolls-Royce.	Entire document
Attachment 2 Rolls-Royce Procedure, System Design (Safety Systems)	8 303 334 F				Entire document

Document Title	Document Number	Part of document sought to be withheld from public disclosure	Basis for proposing the information be withheld, encompassing considerations set forth in § 2.390(a)	Specific statement of the harm that would result if the information sought to be withheld is disclosed to the public	Location(s) in the document of all information sought to be withheld (Notes 1 and 2)
Attachment 3 Rolls-Royce Drawing	3 008 630 A (Sheet 6)	Entire document (see Note 2).	Trade secrets and / or commercial information as per § 2.390(a)(4)	Rolls-Royce would be harmed by disclosure of aspects of its proprietary technical processes for safety system manufacturing. These processes underpin the integrity of ***SPINLINE 3*** software, which is an important competitive advantage for Rolls-Royce.	Entire document

Notes:

(1) As required in NRC Information Notice (IN) 2009-07, documents containing proprietary information are marked with the word "Proprietary" at the top of the first page of the document and at the top of each page containing such information. In proprietary documents, brackets ("[[ ]]") denote proprietary information. In the proprietary document, the two brackets denoting the end of a proprietary segment of a report may appear one or more pages following the bracket indicating the start of the proprietary segment. In a nonproprietary edition of a proprietary document, the material within the brackets is removed.

(2) As noted in IN 2009-07, in instances in which a nonproprietary version would be of no value to the public because of the extent of the proprietary information, the agency does not expect a nonproprietary version to be submitted.

RESPONSE TO REQUEST FOR ADDITIONAL INFORMATION

SPINLINE 3 DIGITAL SAFETY INSTRUMENTATION AND CONTROL PLATFORM

PROJECT NO. 773

General Questions / System Overview

The following request for additional information (RAI) questions address regulatory evaluation criteria for the hardware architecture and description for the SPINLINE 3 Platform. Sections D.1.2 and D.2.2 of Digital Instrumentation and Controls Interim Staff Guidance (Digital I&C-ISG-06) (Agencywide Documents Access and Management System (ADAMS) Accession No. ML110140103) provides guidance on this item.

RAI-1: Per Section D.1.2 of ISG-06, applicants should submit sufficient documentation and descriptions to allow U.S. Nuclear Regulatory Commission (NRC) staff to identify the hardware being used, how the hardware items function, how the various hardware items are interconnected, and any software in the system.

Please provide a specific description of how the SPINLINE 3 components are interconnected. A physical example of the SPINLINE 3 system with a description of how information flows through input board(s), memory locations, backplane(s), processors, a Nervia network and output board(s) (as requested in RAI-4 below) may help facilitate this description.

Rolls-Royce Answer – The response to RAI-1 focuses on physical arrangement of the ***SPINLINE 3*** equipment and the dataflow paths from the input modules through the backplane to the central processing unit and back through the backplane to the output modules. This flow path is representative of input/output (I/O) processing within a single safety division. The response also describes the network connection between a processing unit and its associated communication Station.

The response to RAI-2 focuses on ***SPINLINE 3*** system architectures and associated design constraints. This response discusses how the modular ***SPINLINE 3*** equipment can be arranged as safety divisions within a system and as subsystems within a safety division.

The response to RAI-3 focuses on ***SPINLINE 3*** backplane and NERVIA network communication protocols. The backplane communication protocol drives the dataflow paths described in the response to RAI-1. The network communication protocol drives dataflow paths between central processing unit independently of the backplane busses.

The response to RAI-4 augments the responses to RAI-1 and 3 by elaborating on the internal functionality of the ***SPINLINE 3*** modules.

The response to RAI-5 expands the discussion in the response to RAI-4 by elaborating on the software and firmware used in certain ***SPINLINE 3*** modules.

As some general background information, please refer to Licensing Topical Report (LTR) section 4.3.2.1:

The 19" 6U chassis includes:

- A metallic frame consisting of riveted and bolted parts, galvanized and chromate passivated, designed for electromagnetic protection and mechanical strength.
- Mounting rails for easy insertion and retrieval during maintenance.
- One or two printed circuit backplanes with board connectors. These connectors are equipped with keys matching their associated board types.

The 19" 6U chassis is designed to host the main electronics boards on the front side and complementary boards known as "Interface boards" on the rear side.

- The main electronic boards, plugged from the front of the chassis, provide the function e.g. processing, analog or discrete acquisition, and the displays and controls available to the maintenance staff.
- The Interface boards, plugged from the rear of the chassis, provide the connectors from sensors signals or to actuators control. Theses interfaces provide adequate isolation and electrical adaptations between field signals and the main electronic boards." The boards can also support the following functions: protection (i.e., electromagnetic, overvoltage, and short circuit), test input connections, and safety position monitoring.

Also refer to LTR section 4.3.2.2:

The **SPINLINE 3** 21 slots Backplane Bus fits in the 19" 6U mechanical chassis and hosts a power supply board, a Central Processing Unit (CPU) board and up to 12 digital analog and discrete input and output boards (within the limitations of the power supplies).

The functions of the backplane bus are:

- To provide for the centralization of data acquisition performed by input boards across the Parallel Asynchronous Bus (BAP), whether the input boards use microprocessors or field programmable gate array (FPGA) logic for data acquisition
- To provide for the transmission of output signals established by the UC25 N+ CPU board to the output actuation boards
- To supply power generated by the ALIM 48 V/5-24 V power supply board to the CPU board and to the I/O boards
- To provide connectors to link main electronic boards to their associated Interface boards
- To transmit the I/O boards status (i.e., self-tests) to the UC25 N+ CPU board

The Backplane Bus is a Master/Slave parallel bus with one Master board and one or several Slave boards.

The backplane is available in several sizes with 21, 11, and 10 slots. Two of the smaller backplanes can be installed in a single chassis. The functionalities are the same for the different sizes.

Please note that "backplane bus" refers to the board in the first paragraph of section 4.3.2.2, and to the electronic bus in the second paragraph.

Additional information regarding the BAP

The backplane bus (hardware) is a passive bus that provides interconnection between the processing board and the I/O boards. The main features of the interconnection are the following:

- An electrical parallel bus
- One (and only one) UC25 N+ CPU board controls the backplane bus
- All the other interconnected boards are slaves to the UC25 N+ CPU board (master) and cannot control the bus.

The bus is asynchronous. It addresses the I/O boards by checking the board's address which is wired in the backplane.

The BAP bus interconnects the UC25 N+ CPU board to the different I/O boards. The UC25 N+ CPU board controls the BAP bus with the ***SPINLINE 3*** Operational System Software (OSS), which uses a Rolls-Royce proprietary secure protocol. The BAP bus communication is described further in response to RAI-3 and in LTR Section 4.4. The OSS checks that:

- The UC25 N+ CPU board can communicate with the I/O boards (that the bus address matches the address which is wired in the backplane,
- That any message is transmittable between UC25 N+ CPU board and I/O boards (that the bus data can take both 1 and 0 values on each strand).

Additional information regarding the mechanical arrangement of the backplane

The backplane fits in the middle of the chassis, in between the main boards and the interface boards. Refer to Figures Q1-1 to Q1-3, which illustrate the mechanical implementation principle with the example of a specific ***SPINLINE 3*** rack.

The main boards are connected to the backplane on the front side, whereas the interface boards are connected to main boards through the backplane on the rear side. The backplane has two main separate types of connectors:

- Those that connect the main boards to the BAP bus (XF1).
- And those which connect each main board to its interface board (XF2)

The XF2 connectors are not used for the BAP bus. The backplane panel is a physical and mechanical support for the board connectors. It also supports BAP bus because of its central location. Refer to Figure Q1-4.

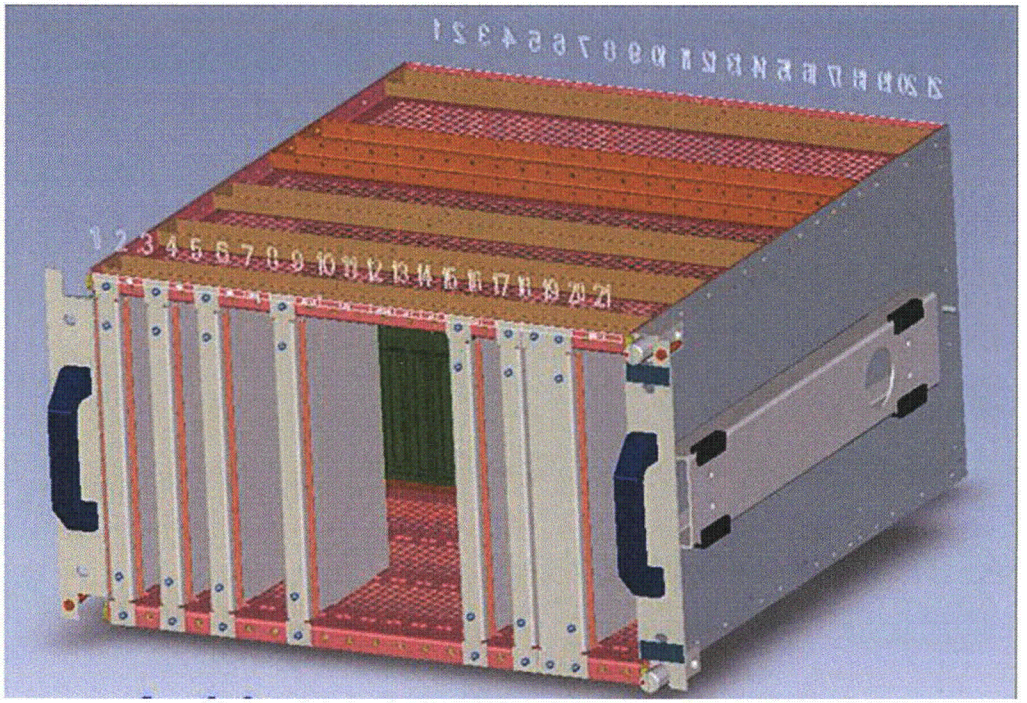

Figure Q1-1: *SPINLINE 3* Chassis - Front View

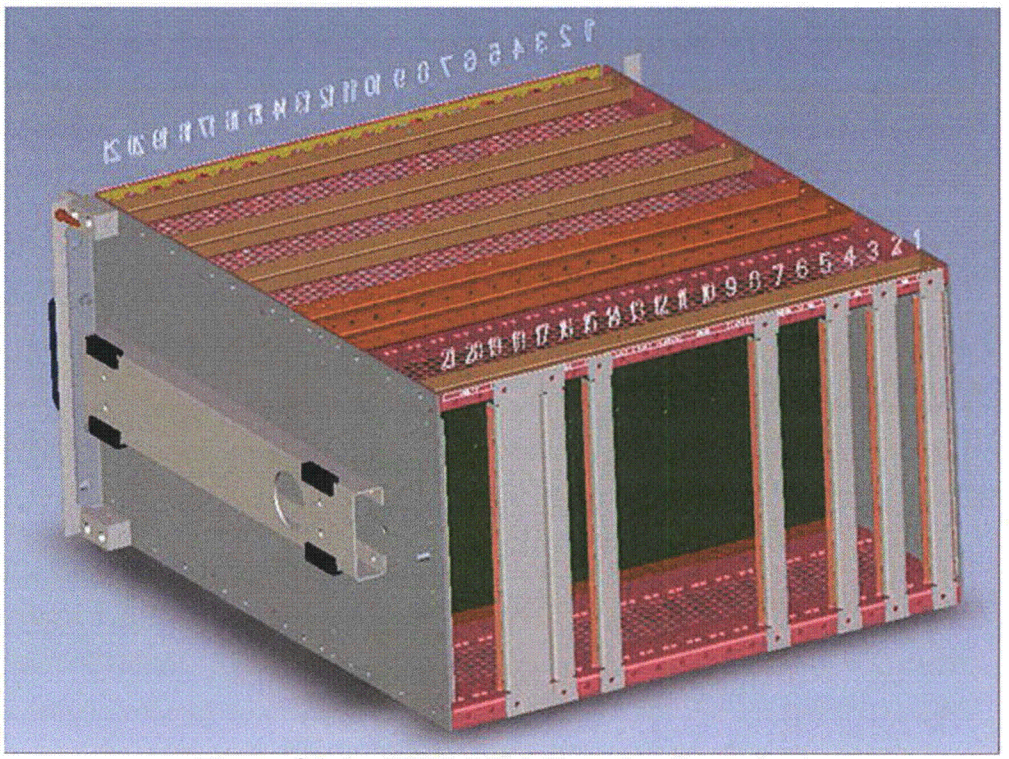

Figure Q1-2: *SPINLINE 3* Chassis - Rear view

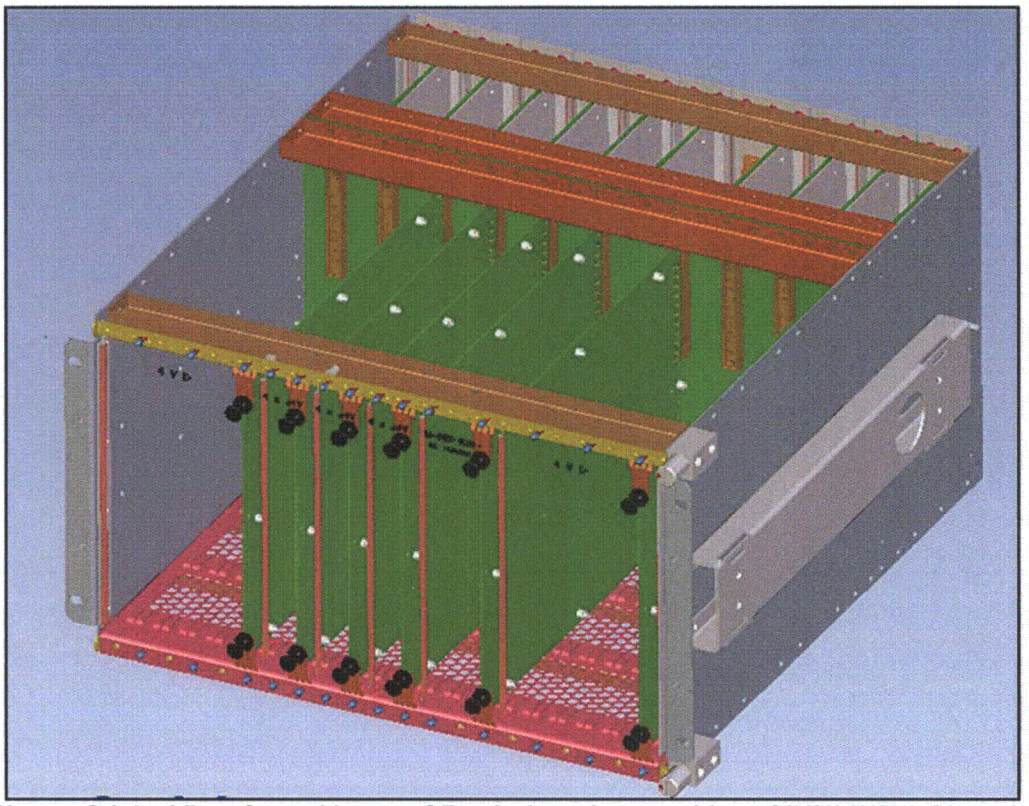

Figure Q1-3: View from Above of Backplane Inserted in a *SPINLINE 3* Chassis

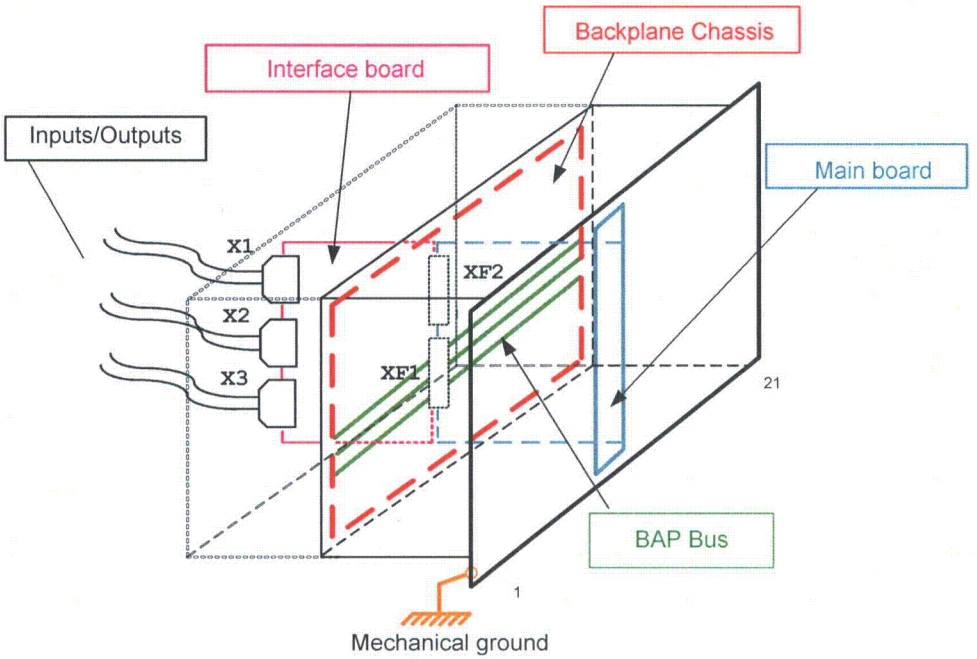

Figure Q1-4: ***SPINLINE 3*** Rack

XF1 connectors are HE 12 / 96 pin fool proof type connectors (H 12D / 32 pins for the power supply); XF2 connectors are HE 12 / 96 pin fool proof type connectors. XC1, XC2, and XC3 connectors (on Figure Q1-5) are power supply board related lugs. Interface boards have standard Sub-D connectors (X1, X2, and X3 on Figure Q1-4) for connection to the rest of the cabinet. The number of Sub-D connectors varies according to the interface board (the 3 connectors on Figure Q1-5 are given as an example).

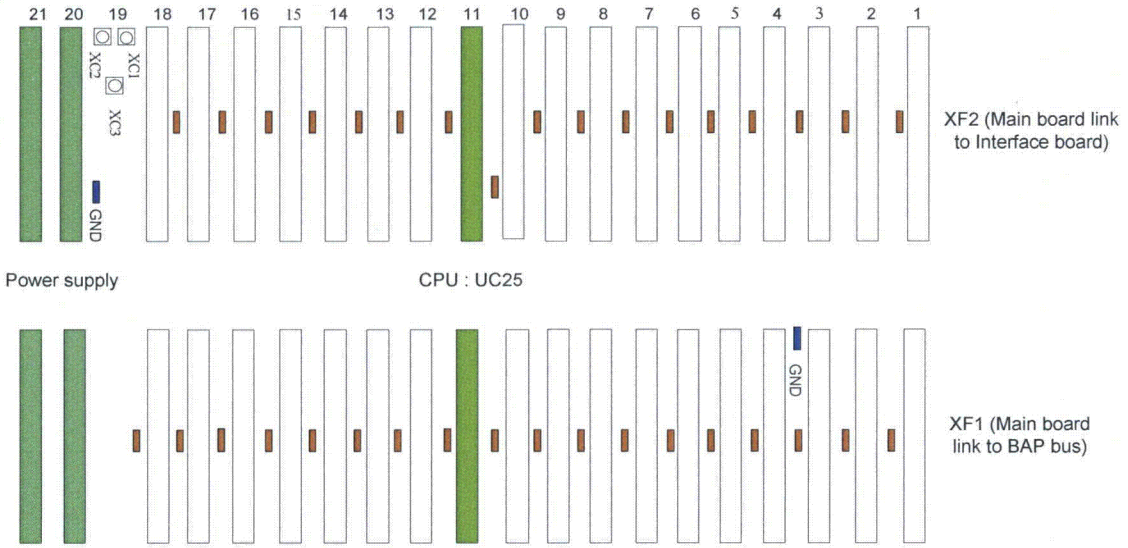

Figure Q1-5: ***SPINLINE 3*** Rack View - Rear

The general I/O dataflow is shown in Figure Q1-6.

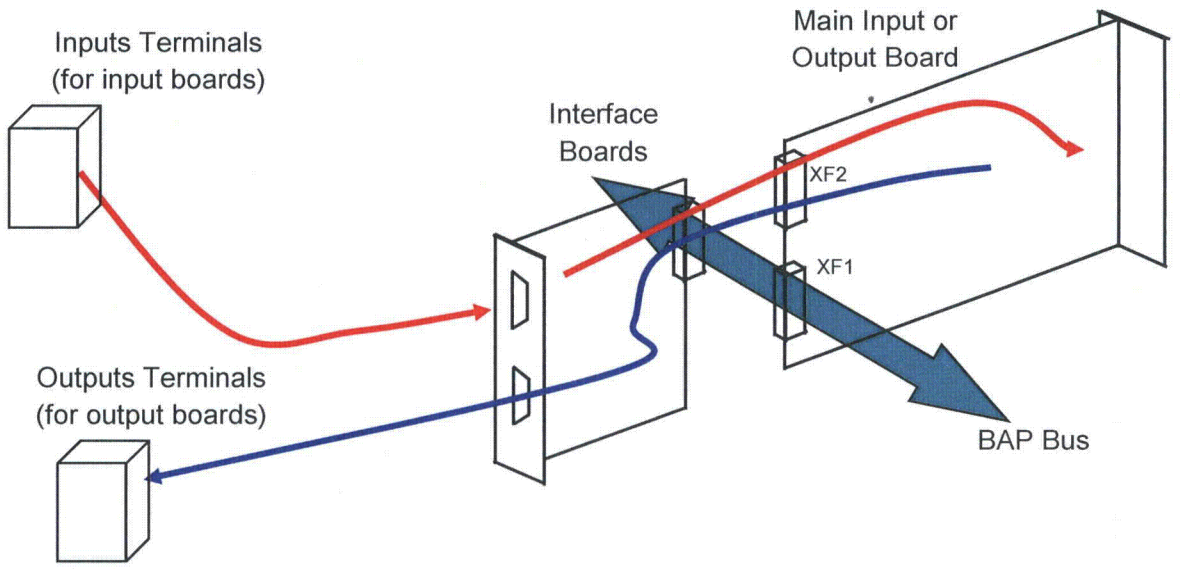

Figure Q1-6: *SPINLINE 3* Dataflow Principles

Input data flow from input boards to the CPU

The inputs from field sensors and equipment are first acquired by an interface board (i.e., I.16EANA, I.32ETOR TI, or I.ICTO interface board). The external field ON-OFF discrete sensors are first routed through the 32ETOR terminal block, which provides the sensor with power supply and provides an initial stage of isolation. The interface boards provide adequate isolation and electrical adaptations between field signals and the main electronic boards. The interface boards also provide standard connection to the rest of the cabinet.

The input signal is then routed to its associated input board (i.e., 16EANA, 32ETOR TI, or ICTO board) through a connector (XF2). The input boards perform signal conversion and conditioning, as described in the response to RAI-4. The input boards communicate with the UC25 N+ CPU board through the BAP bus (via connector XF1). When the input board is addressed by the UC25 N+ CPU board through the address bus, the data acquired by the board and available in the local registers of the board are read by the UC25 N+ CPU board on the data bus. Once acquired the data are stored in the local data memory of the UC25 N+ CPU board, ready to be used by the application software when the application is launched in the software sequenced cycle. Data are considered as valid for the application if all self-test have succeeded, including the correct operation of addressing the board.

The acquisition of field input signals is shown as item 1 on Figure Q1-7. The interface board communication with the input board is shown as item 2. The communication between the input board and the UC25 N+ CPU board is shown as item 3.

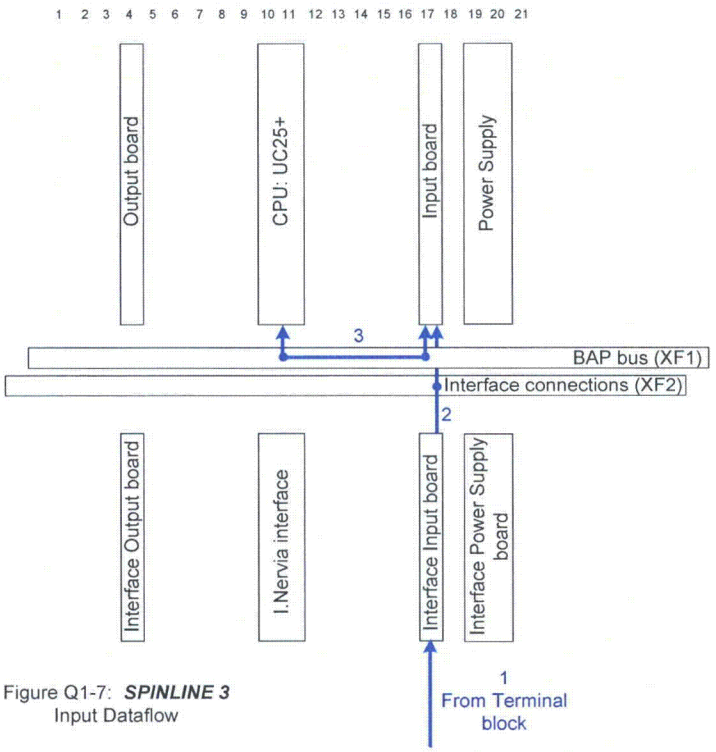

Figure Q1-7: ***SPINLINE 3***
Input Dataflow

Resistance temperature detector (RTD) input conditioning

The 8PT100 conditioning board is installed in a temperature conditioning dedicated chassis with a 21, 11, or 10 slots backplane, with a power supply board. The backplane provides power supply distribution to the board and its interface. The BAP bus on this backplane is not used.

The RTD input signals are acquired by the I.8PT100 Interface board. The interface boards provide Electromagnetic Compatibility (EMC) filtering and RTD wiring connections (e.g., 3 or 4 wire). The signals are then routed to the 8PT100 conditioning board through a connector (XF2). The conditioning board performs signal conversion and conditioning. The resulting signal is then sent back to the interface board. The interface board output signal is then sent to an I.16EANA interface board as an analog input signal. This analog signal is then processed as described above. The I.8PT100 Interface board and 8PT100 conditioning board are discussed further in the response to RAI-4.

The acquisition of RTD field input signals is shown as item 1 on Figure Q1-8. The interface board input communication with the conditioning board is shown as item 2. The conditioning board output communication with the interface board is shown as item 3. The communication between the interface board and the analog input board is shown as item 4.

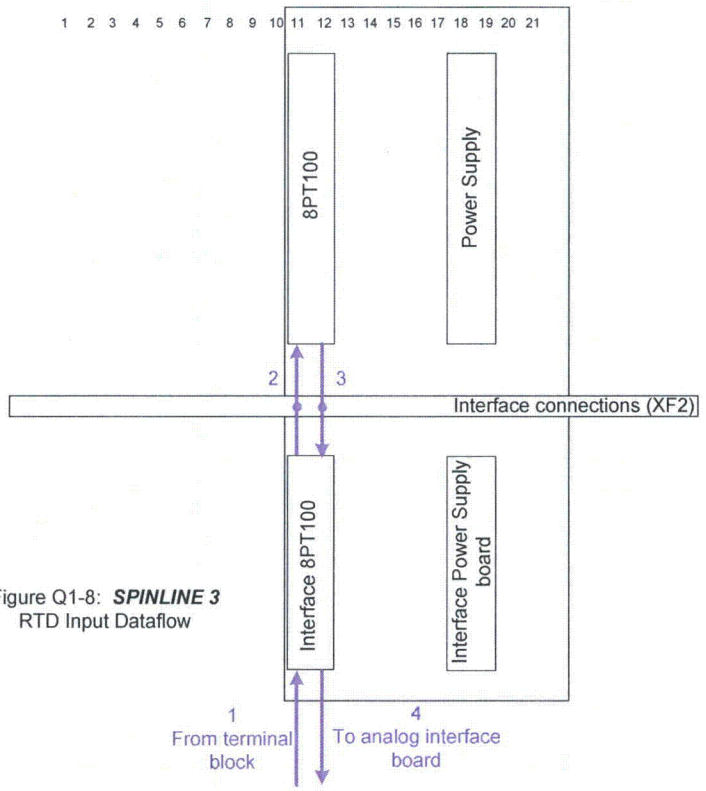

Figure Q1-8: ***SPINLINE 3***
RTD Input Dataflow

Output data flow from the CPU to the output boards

The UC25 N+ CPU board communicates with the output boards through the BAP bus (via a connector XF1). The UC25 N+ CPU board communicates with the output board through the BAP for self testing. The output signals are sent from the UC25 N+ CPU board after processing.

The signal is then routed from the output board (i.e., 6SANA ISO or 32ACT board) to its associated output interface board (e.g., I.6SANA or I.32ACT) through a connector (XF2). The output boards perform signal conversion and conditioning, as described in the response to RAI-4. The 32ACT board communicates with the MV16 Actuator Voting Module and the 8SRELAY Terminal Blocks, as shown in LTR Section 4.3.4.5.

The interface boards provide adequate isolation and electrical adaptations between field signals and the main electronic boards. The interface boards also provide standard connection to the rest of the cabinet. The output boards perform signal conversion and conditioning, as described in the response to RAI-4.

The communication between the UC25 N+ CPU board and the input board is shown as item 1 on Figure Q1-9. The output board communication with the interface board is shown as item 2. The transmission of field output signals is shown as item 3.

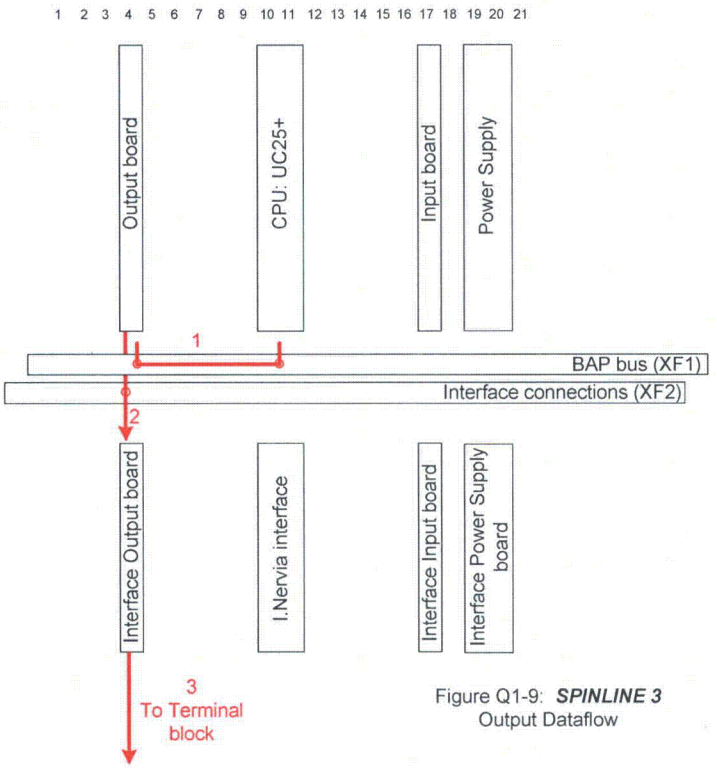

Figure Q1-9: ***SPINLINE 3***
Output Dataflow

CPU communication with the NERVIA network

The UC25 N+ CPU board communicates with the NERVIA network using a NERVIA+ daughter board. The NERVIA+ daughter board is mounted directly onto the UC25 N+ processor board. The NERVIA+ daughter board has no access to the BAP bus. The NERVIA+ daughter board contains dedicated dual port memory, which is used to communicate with the UC25 N+ CPU board. The NERVIA+ daughter board connects directly with the UC25 N+ CPU board. [[

]] UC25 N+ CPU board is connected to an I.NERVIA+ interface board through a connector (XF2). The interface board provides standard connections to the rest of the cabinet and provides electrical isolation. The NERVIA+ daughter board and I.NERVIA+ interface board are discussed further in the response to RAI-4.

The communication between the NERVIA+ daughter board and the I.NERVIA+ interface board is shown as item 1 on Figure Q1-10. The I.NERVIA+ interface board communication with the NERVIA network is shown as item 2. The tenth slot is reserved for the UC25 N+ CPU board.

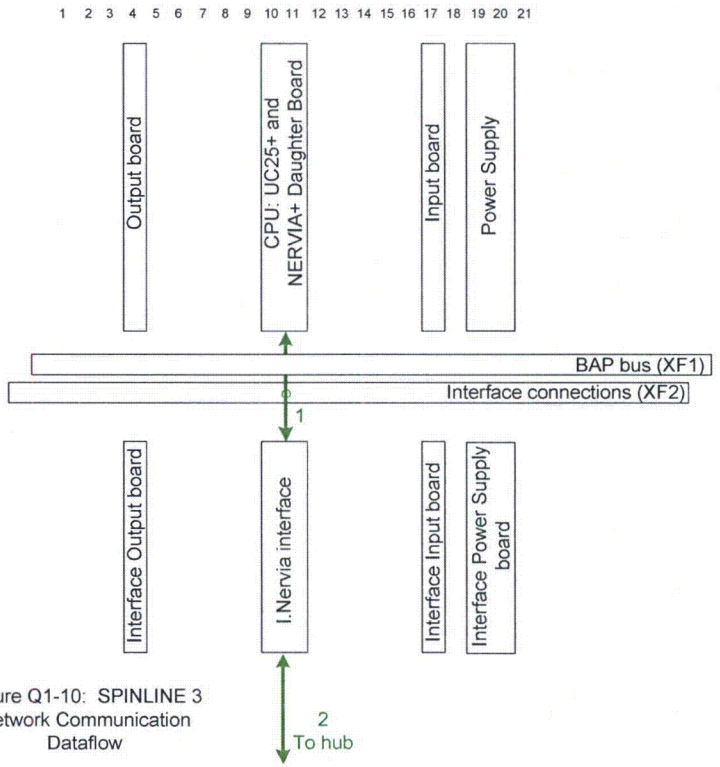

Figure Q1-10: SPINLINE 3 Network Communication Dataflow

The communication path for a single Station is shown in Figure Q1-11. The data flows from the communication processor (MPC 860) on the NERVIA+ daughter board to the I.NERVIA+ interface board through a connector (XF2). The data then flows from the I.NERVIA+ interface board to a NERVIA network hub through a RJ45 connector. The data can then flow to other UC25 N+ CPU boards in the same cabinet through RJ45 connectors to other UC25 N+ CPU boards in different cabinets via fiber optic links. These network arrangements satisfy the network topology criteria in DI&C-ISG-04 Item 14 regarding interdivisional communication. Additional information on NRC DI&C-ISG-04 is provided in LTR Table 3.7-1.

The MPC860 processor on the NERVIA+ daughter board controls the NERVIA network communication with the NERVIA software, which uses a separate Rolls-Royce proprietary secure protocol. The NERVIA communication is described further in response to RAI-3 and in LTR Section 4.5.

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Figure Q1-11: Scheme of NERVIA Components

RAI-2: Related to RAI-1 above, the NRC staff could not determine based upon the licensing topical report (LTR) what restrictions existed regarding design of a physical SPINLINE 3 architecture. Please provide any applicable constraints related to how extensive or complex a SPINLINE 3 architecture could be implemented. For example, how many central processing units (CPUs), input boards, output boards, Nervia boards, Nervia networks, and stations and units on a Nervia network can be implemented in a single SPINLINE 3 system? Are these restrictions/limitations technical or administrative?

Rolls-Royce Answer - The response to RAI-2 focuses on ***SPINLINE 3*** system architectures and design limitations. The requested information is provided for the system, division, and cabinet levels.

The System Level Perspective

LTR Figure 4.2-2 shows a representative (bounding) four division system architecture. The associated text states that safety systems are either typically three or four divisions. The general rule is that the ***SPINLINE 3*** systems will follow the redundancy requirements for the safety system (e.g., can be 2, 3, or 4 division), derived from the plant-specific single failure analysis and Institute of Electrical and Electronic Engineers (IEEE) Std 603 compliance. Single-division architectures may be used in a non-safety system. It is expected that a licensee that implements a ***SPINLINE 3*** digital system in the same redundancy configuration as their existing design and in accordance with the restrictions outlined above would require a minimal review, which confirms that the single failure analysis results are consistent with the plant licensing basis.

Interdivisional communication will only occur at the voter level, as shown in Figure 4.2-1. The underlying technical issues related to independence affecting the NRC review are not dependent on whether a 2-, 3-, or 4-fold redundancy architecture is used. No other architecture configurations are envisioned (e.g., interdivisional communication is not envisioned at the signal processing, trip logic or output signal levels) as an administrative limitation. Any other interdivisional communication schemes used for a project will require a separate NRC review.

The interface between the safety system and non-safety system will always be one way from the Class 1E to non-safety. The underlying technical issues affecting the NRC review are not dependent on whether a 2, 3, or 4-fold redundancy architecture is used. No other architecture configurations are envisioned. No bidirectional communications schemes are envisioned as an administrative limitation. Any bidirectional communication scheme used for a project will require a separate NRC review.

LTR Section 4.3.2.2 describes the smaller backplanes that can be used to have multiple processors in the same cabinet. LTR section 4.2.7 does not preclude different divisions from being housed in the same cabinet. Equipment from different divisions housed in the same cabinet must meet the applicable requirements for physical separation and independence.

The Division Level Perspective

LTR Figure 4.2-1 shows a representative (bounding) division architecture. The associated text outlines various hardware configurations that can be used within a division. [[

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These options do not affect the generic platform features of the ***SPINLINE 3*** system (i.e., the hardware, software, or communications features described in the LTR). Instead, these options only affect certain plant-specific system analysis. The number of serial processing layers within a division can affect the overall system reliability and will affect the overall system response time (e.g., more processors result in longer response times). The use of parallel processing paths with diverse algorithms affects the diversity and defense-in-depth analysis (e.g., additional diversity for certain common mode failure scenarios). The use of redundant voters within a division affects the overall system reliability evaluation. These options do not affect the plant-specific single failure analysis that is satisfied by the divisional redundancy.

The ***SPINLINE 3*** LTR does not seek approval for interdivisional communication above the voting layer to simplify NRC's review for compliance with DI&C-ISG-04 Items 1 and 3 regarding interdivisional communication. Additional information on NRC DI&C-ISG-04 is provided in LTR Table 3.7-1. Any other use of interdivisional communication in a system must be justified on a plant-specific basis.

The inclusion of the display processing functions in LTR Figure 4.2-1 is meant to be illustrative of the one-way communication interface requirements. No Video Display Unit is included in the scope of the LTR and no specific approval is sought for such a device.

It is expected that a licensee that implements a ***SPINLINE 3*** digital system in the same divisional configuration as the existing design and in accordance with the restrictions outlined above would require a minimal review, which confirms that the response time performance and system reliability are consistent with the plant licensing basis.

The Cabinet Level Perspective

The ***SPINLINE 3*** digital system allow for various arrangements of hardware components. The LTR Section 4.3.2.3 describes each of the hardware elements of the generic ***SPINLINE 3*** platform and explains their use. Additional hardware details are available in the hardware data sheets in LTR Appendix B. There are basic rules on how the components are allowed to be connected to build a ***SPINLINE 3*** system.

- Power Supply: Provides power needed by one backplane from the cabinet power supply. There is one power supply board per backplane.
- Master board: UC25 N+ CPU board able to control data exchange on the backplane. Only one UC25 N+ CPU board can be installed in a backplane at a given time. The tenth slot is reserved for the UC25 N+ CPU board.
- Slave boards: Functional I/O boards which provide signal acquisition from sensors and generation of output signals to actuators. These boards cannot perform alone. They need are controlled by a UC25 N+ CPU board through the backplane. As noted in LTR Section 4.3.2.2, the 21-slot backplane can host up to 12 digital analog and discrete I/O boards.
- Communication boards: Functional boards performing data reception and transmission functions.
- Conditioning Boards: Functional boards performing analog signal amplification and shaping. This board provides analog signals to the 16EANA analog input board and can be plugged into the backplane for access to the power supply and to its associated I.PT100 Interface board.
- Interface boards: These are plugged in the rear on the backplane. They are linked to their associated main electronic board through a dedicated connector on the backplane. They do not exchange information through the backplane. The number of interface boards is limited by the number of slots in the backplane.

The backplane is available in several sizes with 21, 11, and 10 slots. Two of the smaller backplanes can be installed in a single chassis. The most common installation is a 21 slot backplane bus installed in a single chassis. As noted above, only one UC25 N+ board can be installed in a backplane at a given time. In the case of a small safety instrumentation and control (I&C) system with a limited number of input and output boards, it may be possible to use the 10 and 11 slot backplanes, each with its own UC25 N+ CPU board and set of input, output and communications boards. The ***SPINLINE 3*** Qualification Test Specimen System Specification (3 006 404 E) describes how the different backplanes are incorporated into the test system.

The general rule is that the number of components in a subsystem is limited by the number of slots in the backplane. One UC25 N+ CPU board is used per Unit. One NERVIA+ daughter board can be mounted on the UC25 N+ CPU board to provide communication Stations for the Unit. The UC25 N+ CPU board uses two slots with or without the daughter board. One power supply module is used and occupies one slot. The total power consumption by the boards must be checked against the power supply capacity. The remaining slots (i.e., 7, 8, or 18) are available for using I/O boards in any combination or number. The RTD I.8PT100 Interface board uses two slots.

The number of chassis and I/O modules need to take into account different parameters for a project:

- mechanical size of the chassis (e.g., up to 6 chassis could be installed in a cabinet if only mechanical sizing was the restriction),
- number and type of I/O connections, which sets the number and type of I/O modules, and
- total power dissipation.

The appropriate sizing is defined during the project design phase by Rolls-Royce. The general constraints for hardware configurations are described in Section 7 of document ***SPINLINE 3*** / OSS / Software Requirement Specification (1 207 108 J), which was submitted to NRC by Rolls-Royce letter dated February 1, 2010.

Equipment Qualification Perspective

The NRC safety evaluation report for EPRI TR-107330 notes that the arrangement of the modules has the potential to change the stresses that occur during seismic and environmental testing. Therefore, the testing should be designed to provide bounding conditions for these stresses. The EPRI TR-107330 test methodology is designed to provide bounding conditions for these stresses and is used as the basis for the ***SPINLINE 3*** qualification program. The ***SPINLINE 3*** Equipment Qualification Plan (3 006 501 D) and associated Seismic Test Procedure (3 010 288 B) and Environmental Test Procedure (3 010 287 B) are based on the EPRI 107330 test methodology and describe a test program that bounds the stresses that occur during seismic and environmental testing.

Regulatory Guide 1.180, Revision 1, describes methods acceptable to the NRC for complying with regulations on testing practices to address the effects of electromagnetic interference (EMI) and radio frequency interference (RFI) and power surges on safety-related instrumentation and control systems. The ***SPINLINE 3*** Equipment Qualification Plan (3 006 501 D) is based on the Regulatory Guide 1.180 test methodology. The EMI/RFI testing ensures that the ***SPINLINE 3*** modules are not an internal source of EMI/RFI problems. The EMI/RFI susceptibility testing ensures that the ***SPINLINE 3*** modules are not vulnerable to external sources of interference. The use of the open frame test specimen for the EMI/RFI testing results in no limitation on the number of ***SPINLINE 3*** modules or their orientation within a rack.

The bounding approach to qualification testing used by Rolls-Royce results in no additional limitations on the ***SPINLINE 3*** modules arranged in a rack.

Network Configuration Limitations

The NERVIA network configuration depends on the following key parameters:
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The number of transmitting Stations on a network and the amount of data transmitted by each Station will determine the overall network cycle time for the system, as described in LTR Section 4.5.2.1. The deterministic nature of the NERVIA protocol satisfies the cycle time criteria in DI&C-ISG-04 Items 5 and 20 regarding interdivisional communication. Additional information on NRC DI&C-ISG-04 is provided in LTR Table 3.7-1. The project-specific system response time requirement is often the limiting factor on network designs.

The number of hubs and converters in a project-specific network must be checked as a plant-specific action item. The overall system response time must be demonstrated to meet the plant-specific safety requirements.

Example ***SPINLINE 3*** System

An example ***SPINLINE 3*** system implementation for a foreign project is shown in Figure Q2-1. The general architecture is quite similar to that used in the US operating reactors. Safety system sensor input data is acquired by ***SPINLINE 3*** equipment (shown as DIS in the figure) and fed to the protections system (shown as DRPS in the figure). The input data is also shared with non-safety control and monitoring systems gateways through appropriate isolations (shown as IDMS, SAS, and RCS in the figure).

An example ***SPINLINE 3*** division level implementation for a foreign project is shown in Figure Q2-2. [[

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The modular nature of the ***SPINLINE 3*** technology provides the flexibility to meet customer performance requirement (e.g., functionality and reliability) and local regulatory requirements (e.g., redundancy, independence, and diversity).

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Figure Q2-1: Example *SPINLINE 3* System Architecture

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Figure Q2-2: Example *SPINLINE 3* Division Level Architecture

RAI-3: Section 4.3.2.2 of the LTR states that the backplane bus gathers and passes data among the input/output (I/O) boards and the CPU. Please describe how the backplane communication is performed. Also, describe the communication between the backplane and the Nervia network, if existent.

Rolls-Royce Answer – The response to RAI-3 focuses on ***SPINLINE 3*** backplane and NERVIA network communication protocols.

The ***SPINLINE 3*** backplane bus (hardware) is a passive bus that provides interconnection between the processing board and the I/O boards. There is no communication between the BAP and NERVIA networks. The backplane is a mechanical support that provides functions (e.g., to support board connectors and support the BAP).

The ***SPINLINE 3*** OSS controls the operation of the backplane bus. The Basic Functions (BF) software modules are used to access the hardware functions, including input and output modules, NERVIA network support, and self-diagnostics, as shown in Figure Q3-1.

The ***SPINLINE 3*** communication bus was developed in the early 1980's. It works as the first generation of system bus. As such, it is built around a communication bus including the address bus, the data bus, and the control bus. The address bus is used cyclically by the OSS to address the boards one by one. The possible addresses allowed for the boards (which are considered as external hardware peripherals) are predefined at code generation and differ from the addresses of other accessible registers of memories mounted on the UC25 N+ CPU board.

The address of a given board, in a given position in the rack, is set during the design phase by a hardwired connection of specific pins on the backplane panel. This address is associated to the location of the board in the rack in its position.

To read or write information to or from a given board, the OSS sets the relevant bits of the address bus. A board is then addressed when the bits on the address bus are equivalent to the address wired on the backplane panel. Addressing and board status are checked during initialization and periodically with self-tests, as described in LTR Section 4.4.3 When the correct address and board status are verified, data corresponding to the inputs or outputs, from/or to the boards, are set by the boards or the OSS on the data bus to be exchanged in the appropriate direction.

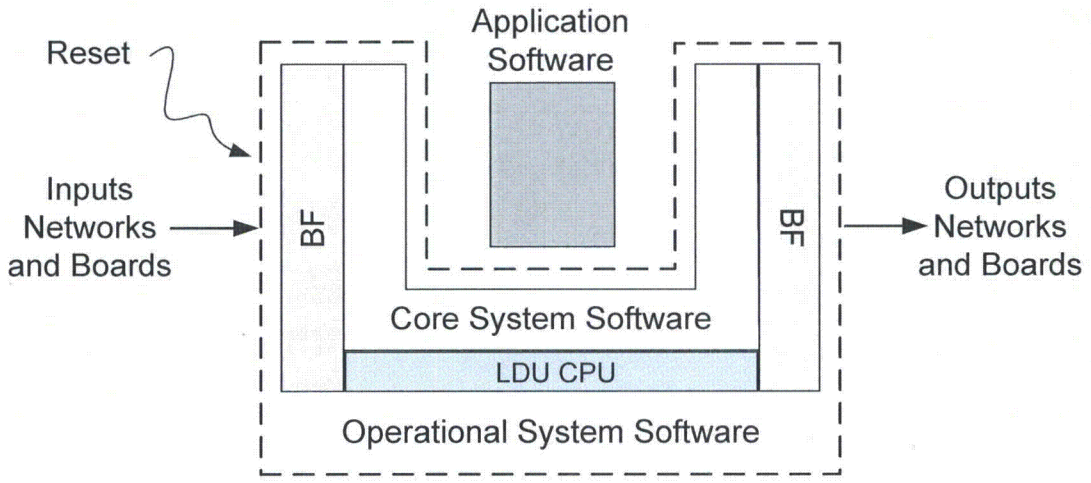

Figure Q3-1: Processing Unit: Hardware / Software Architecture

Input Acquisition

The input function acquires information from each type of input board via the backplane bus. For the 32ETOR, there are up to 32 discrete inputs. For the 16EANA, there are up to 16 analog inputs. For the ICTO pulse acquisition board, there are up to two pulse count inputs. During acquisition, checks are performed on input values, and if an error is detected, the validity of the input is set to "invalid" and the Operation status of the board is set to "fault".

The input function also acquires blocks of data from the NERVIA network, as needed by the application software. Each acquired data item has its own validity, set as described LTR Section 4.4.3.6.4, and transmitted to the application software.

The flow chart of data acquisition is shown in Figure Q3-2.

[[

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Figure Q3-2: Acquiring Information

Output Transmission

The output function transmits information to output boards and networks. This function provides data to the output boards via the backplane bus. The 32ACT board sets up to 32 discrete outputs. The 6SANA board sets up to 6 analog outputs. During transmission, controls has been performed on outputs, and if an error is detected the board is set to "fault".

The output function also transmits blocks on the NERVIA networks to all Units connected to this ***SPINLINE 3*** chassis. It sets all indicators used by receiving Units in order for them to detect possible faults on the transmission channel.

The flow chart of data transmission is shown in Figure Q3-3.

[[

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Figure Q3-3: Transmitting Information

The ***SPINLINE 3*** OSS is described in more detail LTR Section 4.4.

Network Communication

The NERVIA network software function is to transfer data from one UC25 N+ processing units to others, without any modification. NERVIA guarantees the cyclical distribution of data, which is supplied to each communication Station by its UC25 N+ processing unit.

NERVIA is a network dedicated to the exchange of information inside and among divisions of I&C safety systems. NERVIA allows a set of processing Units to permanently exchange a pre-defined set of data within a bounded time frame, in order to ensure deterministic response time of safety actuations under all plant conditions. The basic concept of the NERVIA network is to allow the exchange of data between processing Units as if these data were wired and periodically updated by one Unit and scanned by all others through digital I/O boards.

This exchange of data is such that the same information is sent again and again on the network and that the exchanged values evolve only when external conditions evolve, such as toggle of a discrete input or change in a sensor value. In order to implement this, the NERVIA network is "cyclic", i.e. each Station transmits its information periodically at its turn, and "broadcast" i.e. each transmitted message is received quasi simultaneously by all other Stations on the network. No acknowledge mechanism or answering messages is implemented. Corrupted or missing messages are processed by receiving Stations as invalid until reception of the next valid message. The Consistency Blocks used to exchange data meet the requirements DI&C-ISG-04 Items 6, 7, 12, and 15 regarding interdivisional communication. Additional information on NRC DI&C-ISG-04 is provided in LTR Table 3.7-1.

Each processing Unit can read the information produced by all other processing Units on the same network and can issue its own information to these Units, as if this information was permanently available, and without the need to know that it is exchanged through a digital network. The application software processes information coming from the network the same way as information acquired from or sent to I/O boards.

Figure Q3-4 illustrates the basic architecture for data exchange between a safety Unit (a UC25 N+ processor board) and the NERVIA Station.

[[

]] (see LTR Section 4.5.4.3).

[[

]] An example of a simple NERVIA network is shown in Figure Q1-11.

[[

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Figure Q3-4: Basic Architecture for Data Exchange between a Station and a Unit

The separation of the safety processor (UC25 N+ processor board) and the communication processor (NERVIA+ daughter board) meet the requirements DI&C-ISG-04 Item 4 regarding interdivisional communication. The NERVIA software communication protocol meet the requirements DI&C-ISG-04 Items 2, 8, 11, 12, 13, 16, 18, and 19 regarding interdivisional communication. Additional information on NRC DI&C-ISG-04 is provided in LTR Table 3.7-1.

The ***SPINLINE 3*** NERVIA network and software are described in more detail in LTR Section 4.5.

RAI-4: Section 4.3 of the LTR provides descriptions of electronic components, chassis, backplane, and power supplies that can be used to build SPINLINE 3 system architecture. However, this section does not describe how SPINLINE 3 hardware components function. Please describe how each hardware component works. Specifically, how is data gathered from the field, transferred from the interface board to the main electronic board (through dedicated connectors), processed, and communicated to other components, such as the CPU.

Rolls-Royce Answer – The response to RAI-4 augments the responses to Questions 1 and 3 by elaborating on the internal functionality of the ***SPINLINE 3*** modules.

Conditioning Modules

8PT100 board and I.8PT100 interface board

The 8PT100 board and the associated I.8PT100 interface board are Class 1E components. The 8PT100 board conditions the platinum temperature sensor signal and generates voltage and current signals proportional to the sensor voltage value (without correction for non-linearity).

The temperature conditioning channel processes up to eight PT100 platinum temperature sensors, translating changes in resistance to voltage or current levels. The hardware requires both the 8PT100 input terminal blocks and 8PT100 RTD conditioning boards that acquire a total of eight analog signals from PT100 platinum temperature sensors. The 8PT100 board manages the following functions:

- Supplies the platinum temperature sensors with a bias current
- Conditions the analog input signals from sensors into voltage and current output levels
- Isolates inputs from each other
- signals that the board is in test mode
- provides power at specified voltages from the 24 volt (V) backplane supply

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The 8PT100 board must be implemented with the I.8PT100 interface board. This interface board is installed on the back of the BAP bus.

The I.8PT100 interface board provides the 8PT100 board with input signals from the platinum temperature sensors, provides the output signals from the processing performed by the 8PT100 board, is used to place the 8PT100 in test mode and performs also EMC filtering.

[[

]] This analog board provides analog signals to the 16EANA analog input board. It can be plugged into the backplane for access to the power supply and to its associated I.PT100 Interface board.

Note: The statement in LTR Section 4.3.2.3 should be corrected as noted below:

- **Conditioning Boards:** Functional boards performing ~~low level pulse or~~ analog signal amplification and shaping.

Input Modules

16E.ANA ISO board and I.16EANA interface board

The 16E.ANA ISO board is used to acquire values on 16 differential analog inputs and convert them in sequence into 16-bit digital data available on the BAP.

Any 16E.ANA ISO analog input can be configured independently with its own acquisition range.
[[

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The 16E.ANA ISO board is implemented with the I.16EANA interface board, which performs EMC filtering for all analog inputs, provides connections for periodic tests, and checks the presence of analog input cables on its connectors. [[

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The analog input acquisition hardware also uses a ***SPINLINE 3*** Terminal Block, which is installed outside of the chassis. The 16E.ANA ISO board is installed in the chassis and connects to the front of the BAP bus. This interface board is installed on the backplane.

When 8PT100 RTD conditioning board is used, the 16E.ANA ISO board performs the acquisition of the voltage signals originating from the 8PT100 RTD conditioning board. These signals are acquired in separate isolated groups to maintain isolation provided by the 8PT100 boards.

32ETOR TI SR board and I.32ETOR TI interface board

The 32ETOR TI SR board is used to acquire values on 32 isolated on/off inputs and make the value of each input available on the BAP.

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The I.32ETOR TI board acquires input signals from the sensors and directs these signals to the 32ETOR TI SR board. The interface board also performs EMC filtering and is used to place the 32ETOR TI SR board [[ ]]

[[

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The 32ETOR Terminal Block is installed outside of the chassis. The 32ETOR TI SR board is installed in the chassis and connects to the front of the BAP bus. This interface board is installed on the backplane.

ICTO board and I.ICTO interface board

The ICTO board performs the acquisition of pulses with a count-rate ranging from 1 count per second (cps) up to 6.5 x 10^6 cps. The ICTO board performs the acquisition of two pulse signals. It collects both the number of pulses and the duration of the counting time and forwards these data to the UC25 N+ processor board, which performs the count rate calculation. [[

]] (See response to RAI-5 for more details.)

The ICTO board must be implemented with the I.ICTO interface board. The I.ICTO interface board acquires input signals from the sensors and directs these signals to the ICTO board. The interface board also performs EMC filtering and is used to place the ICTO board [[
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The ICTO board is installed in the chassis and connects to the front of the BAP bus. This interface board is installed on the backplane.

Output Modules

6SANA ISO board and I.6SANA interface board

The 6SANA ISO board performs the digital to analog conversion and the isolation of six outputs. This analog output board can supply the following outputs, based on data sent from the UC25 N+ processor board:
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The 6SANA ISO board is installed in the chassis and connects to the front of the BAP bus. The I.6SANA interface board is installed on the backplane.

[[ ]]

32ACT board and I.32ACT interface board

The 32ACT board has 32 isolated on/off outputs used to control low level relays. The relays are in turn connected to power actuators. All ON-OFF outputs are insulated from each other.

Commands are transmitted by the UC25 N+ CPU board via the BAP bus and an FPGA on the 32ACT board. (See the response to RAI-5 for more information on the FPGA.)

The 32ACT board consists of the following functional sections:
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The I.32ACT interface board comprises EMC filters and [[

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The 32ACT board is installed with the I.32ACT interface board. The 32ACT board is installed in the chassis and connects to the front of the BAP bus. The 32ACT interface board is installed on the backplane.

Processing Modules

UC25 N+ CPU board

The central processing function is implemented with the UC25 N+ CPU board. The UC25 N+ CPU board is installed in the chassis and connects to the front of the BAP bus. The UC25 N+ CPU board performs the processing and control unit functions. It is built around a 25 MHz 68040 Freescale microprocessor CPU board, with two megabytes of read-only flash memory, two megabytes of write-protected random access memory (RAM) for operational system software and application software execution, two megabytes of RAM for data space, and 64

kilobytes of non-volatile Electrically Erasable Programmable Read-Only Memory (EEPROM). The CPU runs the OSS and the Application Software and supported by a 68360 communication coprocessor.

[[

]] The UC25 N+ also manages an asynchronous serial link that is accessed through the front panel RJ45 connectors. This link is used during maintenance, to connect the Local Display Unit (LDU) directly to the UC25 N+ CPU of the processing Unit.

[[ ]] The UC25 N+ CPU board communicates with I/O boards through the BAP bus and with the NERVIA+ daughter board through a dedicated bus.

Note: The statement in LTR Section 4.3.2.3 should be corrected as noted below:

- CPU board: UC25 N+ – based on a MC68040 microprocessor hosting and running the Operational System Software and the Application Software. [[

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The UC25 N+ CPU board is installed in the chassis and connects to the front of the BAP bus. The UC25 N+ CPU board is installed with NERVIA+ daughter board and I.NERVIA+ interface board.

NERVIA+ daughter board and I.NERVIA+ interface board

The NERVIA+ daughter board is mounted directly onto the UC25 N+ CPU board. The daughter board implements the NERVIA digital communications protocol and provides the separation between logic processing and communication processing required by NRC DI&C-ISG-04 item 4 regarding interdivisional communication. Additional information on NRC DI&C-ISG-04 is provided in LTR Table 3.7-1.

[[

]] as described in LTR Section 4.5.3. (See the response to RAI-5 for more discussion on the MPC860 microprocessor and CPLD.)

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The NERVIA+ daughter board requires the use of an I.NERVIA+ interface board.

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The I.NERVIA+ interface board is installed on the back of the backplane, in the slot corresponding to the UC25 N+ CPU board mounted on the front of the backplane.

The NERVIA communications software is described in LTR Section 4.5.

The twelve reliability analysis and predictive safety analysis reports submitted by Rolls-Royce letter dated December 23, 2009 also contain descriptions of the ***SPINLINE 3*** hardware modules (including function block diagrams).

LTR Section 4.3 and Appendix B also contain information on the ***SPINLINE 3*** hardware modules.

Note: The statement in LTR Section 4.3.4.7 should be clarified as noted below:

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RAI-5: Section 4.3 of the LTR states that the following components include electronic sub-components, such as field programmable gate arrays (FPGAs), to process data. For each component and sub-component; describe logic and data processing, process design and development, and how it is addressed under the commercial grade dedication program.

a. Analog Input Board 16EANA ISO – processing implemented using FPGA
b. Calibrated Pulse Acquisition Board ICTO – processing implemented using an Intel 8031 microcontroller
c. Actuator Drive Board 32ACT – processing implemented using FPGA
d. Nervia+ Daughter Board – processing implemented using MPC860 and complex programmable logic device.

Rolls-Royce Answer to Part a) – The Actuator Drive Board 32ACT utilizes an [[

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More information on the functions performed by the 32ACT module can be found in Sections 5 and 6 of Rolls-Royce document 5 100 437 019 C, Reliability analysis and predictive safety analysis: ***SPINLINE 3*** 32ACT board and I.32ACT board. This document was submitted to NRC by Rolls-Royce letter dated December 23, 2009.

The development process used for FPGA-based components is briefly described in LTR Section 6.2.10.

Note: The statement in LTR Section 6.2.10 should be corrected as noted below:

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The 32ACT module was designed to the I&C France Quality Assurance Program applicable to Class 1E hardware, as described in LTR Section 2.1. Roll-Royce established a development process (with associated design and validation instructions) to be used for FPGA development, due to the programmable capability of these components and to their ability to embed potentially complex functions.

[[

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The design process used for the 32ACT module is shown in Figure Q5-1. Additional detail for the associated 32ACT firmware development process is shown in Figure Q5-2.

The following development documents exist (in French) that describe the design and testing of the 32ACT firmware:

- 32ACT FPGA Requirements Specification (5 100 436 536 B)
- 32ACT FPGA Detailed Design Specification (5 100 436 537 A)
- 32ACT FPGA Detailed Design Report (5 100 436 538 B)
- 32ACT FPGA Test Program Specification (5 100 436 539 A)
- 32ACT FPGA Simulation Test Report (5 100 436 540 A)
- 32ACT FPGA Programming Instruction (5 100 436 541 B)

The 32ACT module was also included in the validation testing of the ***SPINLINE 3*** OSS, as documented in ***SPINLINE 3*** / OSS / Software Validation Test Plan (1 207 146 G) and ***SPINLINE 3*** / OSS / Software Validation Test Report (1 207 232 F). These two documents were submitted to NRC by Rolls-Royce letter dated February 1, 2010.

The 32ACT firmware is controlled by the following configuration management procedures (in French):

- Product Identification and Traceability (8 303 221 H)
- Management of Electronic Board Embedding Programmable Components (8 303 436 C)
- Configuration Management during Electronic Development (8 303 711 B)
- Documentation Management of Electronic Sub-Assemblies (8 303 675 F)

The use of a structured design process for the firmware, the robust module type test program, and the integrated validation test with the ***SPINLINE 3*** UC25 N+ hardware and software form the basis for the commercial grade acceptance of the 32ACT module.

Rolls-Royce Answer to Part b) – The ICTO Pulse Acquisition Board includes an Intel 8031 micro-controller. The functions of this micro-controller and the associated embedded software are to:

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More information on the functions performed by the ICTO Pulse Acquisition Board can be found in LTR Section 4.6.8.2.1 and Rolls-Royce document 1 479 513 C, Reliability analysis and predictive safety analysis: ***SPINLINE 3*** ICTO board and I.ICTO interface board. This document was submitted to NRC by Rolls-Royce letter dated December 23, 2009.

The Class 1E software embedded in the ICTO Pulse Acquisition Board was developed according to the life cycle process, configuration management controls, and Quality Assurance Program applicable to Class 1E software that was used for the development of the ***SPINLINE 3*** OSS, as discussed in LTR Sections 6.2.1 through 6.2.8.

The following development documents exist (in French) that describe the design and testing of the ICTO Pulse Acquisition Board software:

- ICTO Software Requirements Specification (1 202 646 D)
- ICTO Software Design Description (1 202 715 C)
- ICTO Software Component Test File (1 202 856 C)
- ICTO Software Integration Test Plan (1 202 812 B)
- ICTO Software Integration Test Report (1 203 102 B)
- ICTO Software Validation Test Plan (1 202 855 B)
- ICTO Software Validation Test Report (1 203 012 C)

The ICTO Pulse Acquisition Board was also included in the validation testing of the ***SPINLINE 3*** OSS, a documented in ***SPINLINE 3*** / OSS / Software Validation Test Plan (1 207 146 G) and ***SPINLINE 3*** / OSS / Software Validation Test Report (1 207 232 F). These two documents were submitted to NRC by Rolls-Royce letter dated February 1, 2010.

The use of a structured design process for the software and the integrated validation test with the ***SPINLINE 3*** UC25 N+ hardware and software form the basis for the commercial grade acceptance of the ICTO Pulse Acquisition Board.

Rolls-Royce Answer to Part c) – The Analog Input Board 16EANA ISO utilizes an Actel FPGA to perform the following functions:

- Interface with the bus
- Interface with the processor (dual ported RAM)
- Control of acquisition (16 inputs in 1 millisecond)
- For each input, processing of the input value for gain and offset adjustment, performed by an Arithmetical and Logic Unit
- Board self-tests

More information on the functions performed by the 16EANA ISO module can be found in Sections 5 and 6 of Rolls-Royce document 5 100 436 348 C, Reliability analysis and predictive safety analysis: ***SPINLINE 3*** 16 E.ANA ISO board and I.16EANA board. This document was submitted to NRC by Rolls-Royce letter dated December 23, 2009.

The development process used for FPGA-based components is briefly described in LTR Section 6.2.10. The 16EANA ISO module was designed to the I&C France Quality Assurance Program applicable to Class 1E hardware, as described in LTR Section 2.1. Roll-Royce established a development process (with associated design and validation instructions) to be used for FPGA development, due to the programmable capability of these components and to their ability to embed potentially complex functions. The design process used for the 16EANA ISO module is shown in Figure Q5-1. Additional detail for the associated 16EANA ISO firmware development process is shown in Figure Q5-2.

The following development documents exist (in French) that describe the design and testing of the 16 E.ANA ISO board firmware:

- 16 E.ANA ISO FPGA Requirements Specification (5 100 435 971 B)
- 16 E.ANA ISO FPGA Detailed Design Specification (5 100 435 972 B)
- 16 E.ANA ISO FPGA Detailed Design Report (5 100 435 992 B)
- 16 E.ANA ISO FPGA Test Program Specification (5 100 435 979 A)
- 16 E.ANA ISO FPGA Simulation Test Report (5 100 436 011 B)
- 16 E.ANA ISO FPGA Programming Instruction (5 100 436 319 B)

The 16 E.ANA ISO module was also included in the validation testing of the ***SPINLINE 3*** OSS, a documented in ***SPINLINE 3*** / OSS / Software Validation Test Plan (1 207 146 G) and ***SPINLINE 3*** / OSS / Software Validation Test Report (1 207 232 F). These two documents were submitted to NRC by Rolls-Royce letter dated February 1, 2010.

The 16 E.ANA ISO firmware is controlled by the following configuration management procedures (in French):

- Product Identification and Traceability (8 303 221 H)
- Management of Electronic Board Embedding Programmable Components (8 303 436 C)
- Configuration Management during Electronic Development (8 303 711 B)
- Documentation Management of Electronic Sub-Assemblies (8 303 675 F)

The use of a structured design process for the firmware, the robust module type test program, and the integrated validation test with the ***SPINLINE 3*** UC25 N+ hardware and software form the basis for the commercial grade acceptance of the 16 E.ANA ISO module.

Rolls-Royce Answer to Part d) – The NERVIA+ Daughter Board – processing implemented [[

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The NERVIA Software is described in more detail in LTR Section 4.5.4.

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The role of the CPLD is described in more detail in LTR Sections 4.5.3 and 4.5.4.3.

More information on the functions performed by the NERVIA+ Daughter Board can be found in Sections 5 and 6 of Rolls-Royce document 1 208 933 C, Reliability analysis and predictive safety analysis: ***SPINLINE 3*** NERVIA+ daughterboard and I.NERVIA+ interface board. This document was submitted to NRC by Rolls-Royce letter dated December 23, 2009.

The Class 1E software embedded in the NERVIA+ Daughter Board was developed according to the life cycle process, configuration management controls, and Quality Assurance Program applicable to Class 1E software that was used for the development of the ***SPINLINE 3*** OSS, as discussed in LTR Sections 6.2.1 through 6.2.8.

The following development documents (in French) exist that describe the design and testing of the NERVIA+ Daughter Board software:

- NERVIA+ Software Requirements Specification (1 208 689 A)
- NERVIA+ Software Preliminary Design Description: Volume 1 - Analysis of Architecture Solutions (1 208 763 A)
- NERVIA+ Software Preliminary Design Description: Volume 2 - Architecture Description (1 208 961 A)
- NERVIA+ Software Detailed Design Description: Volume 1 - Description of Functions (1 208 928 A)
- NERVIA+ Software Design Description (1 208 963 B)
- NERVIA+ Test Strategy Analysis (1 208 879 A)
- NERVIA+ Software Integration Test File (1 208 992 B)
- NERVIA+ Software Validation Test Analysis: Volume 1 - Top Level Document (1 208 910 A)
- NERVIA+ Software Validation Test Analysis: Volume 2 - RequisitePro Report (1 208 956 A)
- NERVIA+ Software Validation Test Report (1 208 985 B)

The development process used for CPLD-based components is briefly described in LTR Section 6.2.10. The NERVIA+ Daughter Board was designed to the I&C France Quality Assurance Program applicable to Class 1E hardware, as described in LTR Section 2.1. Roll-Royce established a development process (with associated design and validation instructions) to be used for CPLD development, due to the programmable capability of these components and to their ability to embed potentially complex functions. The design process used for the NERVIA+ Daughter Board is shown in Figure Q5-1. Additional detail for the associated firmware development process is shown in Figure Q5-2.

The following development documents (in French) exist that describe the design and testing of the NERVIA+ Daughter Board firmware:

- NERVIA+ CPLD Requirements Specification (5 100 436 611 B)
- NERVIA+ CPLD Detailed Design Specification (5 100 436 612 B)
- NERVIA+ CPLD Detailed Design Report (5 100 436 613 B)
- NERVIA+ CPLD Test Program Specification (5 100 436 614 B)

- NERVIA+ CPLD Simulation Test Report (5 100 436 615 A)
- NERVIA+ CPLD Programming Instruction (5 100 436 209 B)

The NERVIA+ Daughter Board was also included in the validation testing of the ***SPINLINE 3*** OSS, a documented in ***SPINLINE 3*** / OSS / Software Validation Test Plan (1 207 146 G) and ***SPINLINE 3*** / OSS / Software Validation Test Report (1 207 232 F). These two documents were submitted to NRC by Rolls-Royce letter dated February 1, 2010.

The NERVIA+ CPLD firmware is controlled by the following configuration management procedures (in French):

- Product Identification and Traceability (8 303 221 H)
- Management of Electronic Board Embedding Programmable Components (8 303 436 C)
- Configuration Management during Electronic Development (8 303 711 B)
- Documentation Management of Electronic Sub-Assemblies (8 303 675 F)

The use of a structured design process for the software and firmware, the robust module type test program, and the integrated validation test with the ***SPINLINE 3*** UC25 N+ hardware and software form the basis for the commercial grade acceptance of the NERVIA+ Daughter Board.

Additional Information on 32ETOR TI SR Board - The 32ETOR TI SR board uses a digital section to [[

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Note: The statement in LTR Section 4.3.2.3 should be corrected as noted below:

- **Slave boards:** Functional boards which provide signal acquisition from sensors and generation of output Signals to actuators. These boards cannot perform alone. They need are controlled by a master board through the backplane bus.
  - Analog input board (ISOlated) 16EANA ISO [[
    ]]
  - Digital isolated input board: 32ETOR TI SR [[

    ]]

The 32ETOR TI SR module was designed to the I&C France Quality Assurance Program applicable to Class 1E hardware, as described in LTR Section 2.1.

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The firmware for the 32ETOR TI SR module was developed in 1998. [[

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The following development documents exist (in French) that describe the design and testing of the 32ACT firmware:

- 5 100 435 511 A, Type Test Procedure for 32ETOR Board
- 5 100 435 512 B, Type Test Report for 32ETOR Board

The 32ETOR TI SR module was also included in the validation testing of the ***SPINLINE 3*** OSS, a documented in ***SPINLINE 3*** / OSS / Software Validation Test Plan (1 207 146 G) and ***SPINLINE 3*** / OSS / Software Validation Test Report (1 207 232 F). These two documents were submitted to NRC by Rolls-Royce letter dated February 1, 2010.

The 32ETOR TI SR firmware is controlled by the following configuration management procedures (in French):

- Product Identification and Traceability (8 303 221 H)
- Management of Electronic Board Embedding Programmable Components (8 303 436 C)
- Configuration Management during Electronic Development (8 303 711 B)
- Documentation Management of Electronic Sub-Assemblies (8 303 675 F)

The use of a structured design process and a robust module type test program, and the integrated validation test with the ***SPINLINE 3*** UC25 N+ hardware and software form the basis for the commercial grade acceptance of the 32ETOR TI SR module.

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Figure Q5-1 : Electronic Module Development Process

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Figure Q5-2 : Firmware Development Process

RAI-6: The LTR does not describe the hardware development process for the SPINLINE 3 platform. As mentioned previously, Section 4.3 of the LTR only describes the hardware components for the SPINLINE 3 platform. Please describe the design and development process for each hardware module and the development process for the SPINLINE 3 platform to be followed for a plant-specific system; in other words, describe how the different hardware components would be assembled to create a safety system. Also, explain if there are rules on how the components can be connected in the SPINLINE 3 platform.

Rolls-Royce Answer – The LTR lists the procedures that govern hardware component development and project-specific design in Table 3.2-1, Item III - Design Control.

Hardware Design Process

Procedure 8 303 349, Definition of the Electronic Design Process, describes the various stages of all design and design-related activities for an electronic circuit board. [[

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The additional design process associated with firmware development is described in the response to RAI-5.

System Design Process

Procedure 8 303 314, Project Development Process, defines the overall design process used for ***SPINLINE 3*** technology development. The overall development process is shown in Figure Q6-1. A ***SPINLINE 3*** project based on an NRC-approved platform will utilize the System Engineering and Software Design processes shown in the figure.

Procedure 8 303 334, System Design (Safety Systems), defines the overall design process used for ***SPINLINE 3*** technology deployment at a nuclear power plant. This procedure defines the process for controlling the design and validation of safety-related I&C systems to meet contractually specified technical and functional requirements, while satisfying quality, cost, and schedule requirements. Procedure 8 307 032, Principle for Control of Design (Safety Systems),

is used to support the design development. Copies of these procedures are provided as an attachment.

The Application Software Development Process for a ***SPINLINE 3*** project is described in LTR Section 6.4. The Application Software Development will be performed in accordance with Procedure 8 303 350, Control of Software Design (Safety Systems). A copy of this procedure was provided to NRC by Rolls-Royce letter dated December 23, 2010.

The rules on how the components can be connected in the ***SPINLINE 3*** platform are described in the response to RAI-2.

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Figure Q6-1: *SPINLINE 3* Technology Development Process

RAI-7: Section 4.3.4.4 of the LTR states the accuracy and the response time of the ICTO board can be adjusted according to the needs. Please explain how these can be adjusted and how these will be evaluated and decided for a plant-specific application.

Rolls-Royce Answer – The ICTO board operates [[

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RAI-8: Section 4.3 of the LTR does not describe the Local Display Unit and the Operator Panel of the SPINLINE 3 platform. Please describe these components and how they are intended to be used in a plant-specific application, including all operating, maintenance, and testing modes.

Rolls-Royce Answer – A description of the ***SPINLINE 3*** LDU and the Operator Panel components and how they are to be used in a plant-specific application is provided below:

Local Display Unit - The LDU is implemented on a laptop personal computer (PC), dedicated to this function. The LDU is not permanently installed. It is connected to the front panel of the UC25 N+ CPU board of a processing Unit by a maintenance staff, for the duration of a maintenance operation, and after having disabled the division or part of division to which this processing Unit belongs.

Setpoint value adjustments may be needed during a reactor operating cycle or between cycles. These adjustments are made using a LDU. The LDU allows the operator to display values of parameters and to make modifications. The only modifications allowed are to parameters which have been defined as modifiable during the design phase. The parameter values are stored in an EEPROM on the UC25 N+ CPU board. It also allows an operator to display selected values and to modify EEPROM-stored parameters, if required by the customer.

The only modifications possible during operation are modifications to parameters which have been defined as modifiable during the design phase. (Note: The processing Unit software cannot be modified by the LDU). The allowed changes are made under strict administrative control and in accordance with the plant-specific Technical Specifications. The affected equipment is considered inoperable and may be bypassed or disabled (as required by the Technical Specifications). Only one Unit is tested at a time, based on requirements in administrative procedures.

The UC25 N+ manages an asynchronous serial link that is accessed through the front panel RJ45 connectors. This link is used during maintenance to connect the LDU directly to the UC25 N+ CPU board of the processing Unit.

The Local Display Unit driver (LDU CPU) manages communication between the LDU and the UC25 N+ CPU board of a processing Unit through an asynchronous serial link. The OSS manages the data exchange with the LDU. The human machine interface (HMI) functions performed by the LDU reside on the LDU. The general hardware and software architecture of a ***SPINLINE 3*** processing Unit is shown in LTR Figure 4.4-1.

The LDU interface function performs the following:

- When no LDU is connected, the LDU interface function is idle.
- When a LDU is connected,
  - It copies value of parameters, inputted by an operator through the LDU HMI, into the EEPROM and into the related data RAM working area; and
  - It transfers parameter values requested by the operator to the LDU for display.

These modifications are performed through the ***SPINLINE 3*** Operational System Software (OSS), which uses a Rolls-Royce proprietary secure protocol.

When an operator modifies a parameter through the LDU, UC25 N+ CPU processing is stopped in the affected equipment. It starts again after the data are saved and the modification is complete.

The LDU interface function remains active in the "Totally Degraded" mode of operation to allow the plant staff access to extract diagnostic information.

Self tests N4, N5 and N14 (described in LTR Section 4.4.3.6.1) relating to the EEPROM are not performed when changes are being made to the EEPROM by the LDU. Test N5 (checksum) is restarted from the beginning when the change made by the LDU or remote operation has been completed, since this self-test spans several cycles.

The design and defined operation of the LDU satisfies the protection from alteration criteria in DI&C-ISG-04 Item 10 regarding interdivisional communication.

Additional information on the LDU can be found in LTR Sections 4.1.3, 4.3.4.7, 4.4.2, 4.4.3.5.5, 4.4.4.3, and 4.6.3. Additional information on NRC DI&C-ISG-04 is provided in LTR Table 3.7-1.

Note: The statement in LTR Section 4.6.3 should be corrected as noted below:

A connecting socket is available in front of each UC25 N+ CPU board to give the operator the possibility to read or modify internal parameters by using the local display unit (LDU). This feature is mainly used during validation tests and ~~not during periodic tests~~periodic verification of the internal parameter settings.

Note: The statement in LTR Section 4.4.4.3 should be corrected as noted below:

As described in Section 4.6.3~~4.4.3.5.2~~, such changes are made under strict administrative control and in accordance with the plant-specific Technical Specifications.

Operator Panel - The Operator Panel is the ***SPINLINE 3*** platform human interface feature used to support periodic testing and maintenance activities. The Operator Panel provides the plant maintenance staff with the necessary connectors, lamps, and pushbuttons to support local monitoring and control for the output inhibition function. The Operator Panel is not used during normal operation of the ***SPINLINE 3*** equipment.

The Operator Panel is a plant-specific and is customized to match cabinet contents and meet customer requirements. The Operator Panel is designed and manufactured using typical components qualified for IE applications. The Operator Panel used for the Qualification Test Specimen (QTS) is shown in Rolls-Royce Drawing 3008630 (sheet 6). A copy of this drawing is included as an attachment.

- PB1 – This pushbutton is used to inhibit one half of the Discrete Signal Generation Logic shown in System Specification Figure 5.
- PB2 – This pushbutton is used to inhibit the other half of the Discrete Signal Generation Logic
- PB3 – This pushbutton is used to reset the inhibit function. This feature is the RESET pushbutton described in the qualification test procedures.
- HL1 and HL2 – Cabinet power indication lights
- HL3 - Inhibit indicator light energized when PB1 is pushed.

- HL4 - Inhibit indicator light energized when PB2 is pushed.
- X1 and X2 – Connectors used to connect the Automated Testing Units

The three main functions of the Operator Panel are:

- Periodic Testing: this function allows the operator to plug in an automatic tester which simulates/reads all inputs/outputs of the equipment
- Inhibition: this function allows the operator to force outputs to a specific status by powering off the corresponding output relays
- Reset: this function restores power to the corresponding output relays

Periodic Testing

The periodic tests described in LTR Section 4.6.7 are performed with ATUs, as described in Section 4.6.9. The ATU is plugged in the front of the tested cabinet. The tests are automatically processed after a manual starting control. The main objective is to detect hardware failures on all the protection signal paths.

The ATU performs the following functions during periodic tests:
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Prior to performance of the periodic tests on a Unit, the Unit shall be placed in a bypass mode by the maintenance operator, in order to avoid any spurious actuation during the periodic test. The bypassed status is signaled to the operator in Control Room. The bypassed status of a Unit is taken into account by other Units as appropriate (typically, the bypassed status of a trip logic Unit in a division is taken into account by the voting logic in the other divisions as expressed in LTR Section 4.2.5).

Inhibition

The MV16 module described in LTR Section 4.3.4.5 includes a feature for inhibition of the control signal to the output relays. LTR Figure 4.3-3 shows an example of the Inhibition Interface. The Inhibit function is actuated from the Operator Panel to support maintenance and testing activities. The conditions for implementing such an inhibition are plant-specific and are defined at the system level.

Actuation of the Inhibit pushbutton results in the following types of actions:
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The maintenance operator cancels the inhibition by pressing the "inhibition reset" push-button.

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Reset

The Reset function removes power to the Inhibit seal-in relay and restores power to the corresponding output relays.

Quality Assurance

The following questions are presented with regard to the Rolls-Royce Civil Nuclear (RRCN) activities related to Part 50 to Title 10 of the *Code of Federal Regulations* (10 CFR), Appendix B.

RAI-9: Related to the evaluation of RRCN's compliance with the provisions of 10 CFR Part 50, Appendix B, reference is made in Section 1.4.1 of the LTR to "an audit by the firm Global Quality Assurance," but no details or reference is provided.

Please provide details for this report related to:

a. When was this audit conducted?
b. What was the scope of the audit?
    - Was the implementation of the Appendix B program to the SPINLINE 3 platform included in the scope of the audit?
c. Is there a reference or documentation available describing the plan and results for the audit?

Rolls-Royce Answer - The audit was carried out January 19 – 23, 2009. The scope was the Design and Manufacture of safety Instrumentation and Controls Systems. The audit was programmatic and addressed the processes and procedures that are used for ***SPINLINE 3***. Yes, there is an audit report dated February 3, 2009 issued by Global Quality Assurance, Inc. The document was submitted to NRC by Rolls-Royce letter dated July 6, 2011.

Commercial Grade Dedication

The following questions are regarding commercial grade dedication under the Electric Power Research Institute (EPRI)-106439 process.

RAI-10: Related to the critical physical characteristics of the SPINLINE 3 platform:

a. In the Master Configuration List (MCL) document (Revision D), the NRC staff could not readily identify what (if any) components belonged to the 8PT100 input terminal or the PCI Nervia+ board that are identified in Table 4.3-1 of the LTR. [Note: These components may be listed, but under some other part identifier that NRC staff could not readily associate with the LTR hardware.] Please verify that those parts are captured in the MCL document (or explain why not).
b. The MCL document (Revision D) lists TS1 and TS2 Manufacturing Files as part of the controlled software items. What are the TS1 and TS2 Manufacturing Files? The NRC staff could not readily associate those items with a SPINLINE 3 component in the LTR.
c. The equipment data sheet in Appendix B of the LTR identifies, but does not describe, any equipment data for the power supply chassis. Please explain where this information is maintained.
d. In the LTR Appendix B equipment data sheets, the 10MBps Ethernet Hub: 3TP/2FL, the Twisted-pair to fiber optic (TP/FL) converters, and MICROSENS TP/FL Converter do not have environmental parameters identified. Please explain the reason for excluding this information?

Rolls-Royce Answer to Part a) - The 8PT100 board (Part Number 5 100 436 479 F) and its input terminal I.8PT100 (Part number 5 100 436 543 D) are listed on page 7 of the Master Configuration List. The PCI NERVIA+ board (Part Number CAR0000064) is installed in non-Class 1E equipment to establish the interface between a Personal Computer and a NERVIA+ network. The PCI NERVIA+ board is installed in a PCI slot in the Monitoring and Maintenance Unit (MMU) and in the ATU (Reference ***SPINLINE 3*** LTR Section 4.3.3). The Master Configuration List for the ***SPINLINE 3*** Qualification project is intended to provide the baseline configuration of the qualified ***SPINLINE 3*** digital safety I&C platform. The PCI NERVIA+ board is not uniquely listed in the Master Configuration List because it is not a qualified component. It is included in the Data Acquisition System (DAS) PC and PXI rack (part number INF0000035C) listed on 16 of the Master Configuration List.

Rolls-Royce Answer to Part b) - Information on the Software Manufacturing File can be found in Section 6.4.9 of the ***SPINLINE 3*** LTR. TS1 is the Test Specimen Application Software of PU1 (TSAP1); TS2 is the Test Specimen Application Software of PU2 (TSAP2).

Rolls-Royce Answer to Part c) - For the 120 V AC/48 V DC and 48 V DC/48-24 V DC power supply chassis, one must refer to the manufacturer technical datasheets, as noted on page 466 of the ***SPINLINE 3*** LTR. Two of the Rolls-Royce part numbers are incorrect. The correct part numbers are:

3 008 767: *converter from 48 V DC to 24 V DC (2 outputs) (manufacturer part number: CP2660-7RD)*
3 008 768: *converter from 48 V DC to 24 V DC (4 outputs) (manufacturer part number: CP4660-7RD)*
3 008 467: *converter from 120 V AC to 48 V DC (manufacturer part number: LK5660-9RDTKB1)*

See the attached manufacturer technical datasheets for details.

Rolls-Royce Answer to Part d) - The information was not included on the datasheets because it was public commercial information that was to be formally established by the qualification testing.

See the attached manufacturer technical datasheets for details.

RAI-11: Related to the critical performance characteristics of the SPINLINE 3 platform:

a. As described in EPRI-106439 and clarified in Generic Letter 91-05, critical performance characteristics are to be identified for the system undergoing commercial grade dedication (CGD). The CGD plan and report submitted for NRC staff evaluation both identify Chapters 4 and 6 of the LTR as containing the critical performance characteristics for the SPINLINE 3 system. In addition, the requirements specification, design description, and interface specification are also credited as identifying the critical performance characteristics. However, these documents do not specifically call out any particular set of items with the terminology "critical performance characteristics." Therefore, the NRC staff must assume that the entirety of these references is considered to be critical performance characteristics, each of which is verified as part of your CGD process. Please elaborate your intentions as to whether only a subset of the material contained in these references is to be considered as critical performance characteristics.

b. The CGD report (Section 5) notes that Methods 1, 2, and 4 (per EPRI-106439 and EPRI NP-5652) were used to verify the adequacy of the various critical characteristics. EPRI-106439 specifically notes that all three of these methods are typically appropriate for verifying the critical performance characteristics. Please clarify how these methods were employed to verify the critical performance characteristics of the SPINLINE 3 platform? [Based upon the dedication acceptance criteria and associated actions described in the CGD report, it is not clear what methods were employed and/or what evidence was generated by RRCN to document that each critical characteristic is traceable to specific verification action(s).]

    i. Method 1 involves special tests and inspections. Describe what combination of tests and inspections were performed to verify each of the critical characteristics identified. Describe what documentation exists that traces each critical characteristic to the special tests and/or inspections performed to verify it. Describe where this evidence is maintained.

    ii. Describe how Method 2 was employed. Provide evidence that documents RRCN's efforts with regard to performing a Commercial Grade Survey.

    iii. Table 2.3-1 identifies the installation history of the SPINLINE 3 platform (and its predecessor platforms from which it evolved). With respect to verifying critical performance characteristics via Method 4, please explain how this information was used in establishing an acceptable item performance record. Provide a description of the operational history of specific components or software (if any) from previous generations of the SPINLINE 3 platform that are relevant to the current SPINLINE 3 platform. Describe what administrative mechanisms have been established to obtain performance data from these platforms. Describe how this data is recorded and maintained. Describe what the RRCN findings were with regard to the operational history of the critical performance characteristics of the SPINLINE 3 platform.

Rolls-Royce Answer to Part a) - *SPINLINE 3* LTR Sections 4.1 through 4.6 describe the critical platform (hardware and software) design characteristics for the ***SPINLINE 3*** technology.

SPINLINE 3 LTR Sections 6.2 and 6.3 describe the critical design process characteristics for the development of the ***SPINLINE 3*** OSS. Section 6.1 provides background information on that development process. Section 6.4 describes the development process for Application Software that would be used for future ***SPINLINE 3*** projects.

The information on the secure development and operational environment in Sections 4.7 and 6.5 has been superseded by the documents provided to the NRC on June 30, 2010.

The response to Part b) below describes how critical performance and dependability characteristics for acceptance were verified using Method 1 and Method 2 techniques.

The Rolls-Royce commercial grade dedication effort for the ***SPINLINE 3*** platform was performed using the NRC-approved guidance of EPRI TR-106439, which is based on the NRC-approved guidance in EPRI NP-5652. This set of guidance provides the overall framework for the technical basis for acceptance and the specific methods used to establish acceptance. It is important to understand how this guidance relates to the use of testing in the acceptance review. Testing can be used to support acceptance in three distinct ways, each with its own set of rules.

Method 1 – EPRI NP-5652 Section 3.1.2 states that "Method 1 should be used when the purchaser desires to verify critical characteristics after the item is received." Method 1 testing is performed during the commercial grade dedication process. EPRI NP-5652 Section 2.5 specifies that this work must be performed in accordance with a 10 CFR 50, Appendix B program.

Method 2 - EPRI NP-5652 Section 3.2.2 states that "Method 2 should be used when the purchaser desires to accept commercial grade items based on the merits of a supplier's commercial quality controls. These controls may constitute quality programs, procedures, or practices." EPRI NP-5652 Section 3.2.3 states that "Two basic criteria must be met when conducting a commercial grade survey. The purchaser must confirm that the selected commercial grade item's critical characteristics are controlled under the scope of commercial quality system activities. The purchaser must also be reasonably assured that the commercial supplier's activities adequately control the commercial grade items supplied." EPRI NP-5652 Table 3-1 lists typical supplier controls that can be surveyed using Method 2, which includes testing. Similarly, EPRI TR-106439 Figure 3-2 shows a review of vendor testing as an element of the dedication process. EPRI NP-5652 Section 2.5 specifies that the review for acceptance of vendor testing must be performed in accordance with a 10 CFR 50, Appendix B program; however, the vendor testing itself is not performed in accordance with a 10 CFR 50, Appendix B program.

Method 3 - EPRI NP-5652 Section 3.3.1 states that "Method 3 involves the verification of critical characteristics by witnessing quality activities before releasing the item for shipment." EPRI NP-5652 Section 2.5 specifies that the verification for acceptance of vendor testing must be performed in accordance with a 10 CFR 50, Appendix B program; however, the vendor testing itself is not performed in accordance with a 10 CFR 50, Appendix B program.

Rolls-Royce performed a review of the historical development records for the ***SPINLINE 3*** platform as part of the commercial grade dedication effort and made two broad conclusions. First, Rolls-Royce concluded that additional testing would be needed to satisfy the US regulatory requirements for hardware qualification. These hardware qualification tests represent Method 1 activities and are described in LTR Section 5.1. Second, Rolls-Royce concluded that the ***SPINLINE 3*** software and firmware development processes (including the original validation testing) were of acceptable based on the rigor of the development processes, quality of the development documentation, and the validity of the results obtained. The software validation tests were accepted by Method 2 and are described in LTR Sections 6.2 and 6.3.

Method 3 was not used by Rolls-Royce for the SPINLINE 3 commercial grade dedication effort. A Method 3 process, if used, would be akin to a licensee observing a factory acceptance test for a system they purchased.

The Rolls-Royce use of Methods 1 and 2 are further described below.

Rolls-Royce Answer to Part b) - Table A-1 in the Dedication Report for the Generic ***SPINLINE 3*** Digital Safety I&C Platform (3 010 795 A) maps the dedication elements of EPRI TR-106439 to the applicable ***SPINLINE 3*** documentation. Additional information on the use of Methods 1, 2, and 4 are described below.

Rolls-Royce Answer to Part b) item i - The ***SPINLINE 3*** Qualification Plan (3 006 501 D submitted to NRC by Rolls-Royce letter dated June 15, 2010), which is based on EPRI TR-107330, identifies qualification testing to verify critical performance characteristics. These tests represent the Method 1 activities that are used in the commercial grade dedication process for the ***SPINLINE 3*** platform. The ***SPINLINE 3*** qualification program is summarized I LTR Section 5.1.

The high level critical performance characteristics for acceptance to be validated through the ***SPINLINE 3*** qualification testing are summarized below:

- The ***SPINLINE 3*** QTS will continue to function correctly during and/or after exposure to abnormal environmental conditions (i.e., incident gamma radiation, temperature, and humidity).
- The ***SPINLINE 3*** QTS will continue to function correctly during and after exposure to Operating Basis and Safe Shutdown Earthquake seismic events.
- The ***SPINLINE 3*** QTS will continue to function correctly during and after exposure to EMI/RFI, voltage surges, and electrical fast transients.
- The ***SPINLINE 3*** QTS will continue to function correctly during and after exposure to electrical faults applied to selected external interface points.

The ***SPINLINE 3*** Qualification Plan identifies the safety functions to be demonstrated by the qualification testing during normal and abnormal operating conditions as follows:

- Proper response of inputs to applied input signals,
- Proper response of outputs to application program control,
- Proper control of connected output devices,
- Proper operation of communication interfaces,
- Acceptable input/output accuracy,
- Acceptable response time,
- Proper response to momentary interruption of input power,
- Proper response to loss of input power,
- Proper response to input power quality (voltage and frequency) variations,
- Proper failover to redundant components.

The qualification tests inherently test the basic functionality of the ***SPINLINE 3*** OSS, TSAP, and NERVIA communication software and the component firmware and software operating within the QTS hardware environment.

The Operability Test Procedure (3 010 295 B submitted to NRC by Rolls-Royce letter dated June 15, 2010) defines specific critical performance characteristics for acceptance that are verified for the various test sequences. These critical performance characteristics for acceptance are summarized below:

- Analog Input and Output Accuracy, to demonstrate no degradation in the accuracy of analog input and analog output circuits.
- Response Time, to demonstrate no degradation in the response time of the digital hardware, as indicated by a change in outputs in response to a change in inputs.
- Discrete Input Operation, to demonstrate no degradation in discrete input circuit voltage switching levels.
- Discrete Output Operation, to demonstrate no degradation in operation and load capability of relay output circuits.
- Timer Function Accuracy, to demonstrate no degradation in hardware implementation of software timer functions.
- Failover Performance, to demonstrate no degradation in automatic failover to redundant components.
- Loss of Power performance, to demonstrate no degradation in capability to fail to a known state on loss of power.
- Power Interrupt Performance, to demonstrate no degradation in capability to operate through momentary input power interruptions.
- Power Quality Tolerance, to demonstrate no degradation in capability to operate under degraded input power voltage and frequency conditions.

Operability Testing is performed at the following times during hardware qualification testing:

- At the completion of Radiation Exposure Withstand Testing
- At the completion of the high temperature, high humidity phase of Environmental Testing
- At the completion of the low temperature phase of Environmental Testing
- At the completion of the low humidity phase of Environmental Testing
- At the completion of Environmental Testing
- At the completion of Seismic Testing

The Prudency Test Procedure (3 010 296 B), which was submitted to NRC by Rolls-Royce letter dated June 15, 2010, also defines specific critical performance characteristics for acceptance that are verified for the various test sequences. These critical performance characteristics for acceptance are summarized below:

- Burst of Events Performance, to demonstrate no degradation in capability to process rapidly changing inputs.
- Communication Port Failure Performance, to demonstrate no degradation in performance during conditions of simulated electrical faults on connected communication ports.

The qualification tests also inherently test the basic functionality of the ***SPINLINE 3*** OSS, TSAP, and NERVIA communication software and the component firmware and software operating within the QTS hardware environment.

Prudency Testing is performed at the following times during hardware qualification testing:

- At the completion of Radiation Exposure Withstand Testing
- At the completion of the high temperature, high humidity phase of Environmental Testing
- At the completion of Seismic Testing
- During Performance Proof Testing

Other critical characteristics for acceptance for ***SPINLINE 3*** OSS, TSAP, and NERVIA communication software and the component firmware and software operating within the QTS hardware environment were specified as correct performance of the system. These verifications demonstrate correct operation of the ***SPINLINE 3*** software operation, as shown in LTR Figures 4.4-2 through 4.4-9. The critical characteristics for acceptance to demonstrate normal operation of the ***SPINLINE 3*** software include:

- Successful initialization
- Transition to cyclical mode
- Execution of self-diagnostic tests to detect and signal failures in the hardware environment
- Cycle time management maintaining a fixed cycle time (absence of halts due to cycle time being exceeded)
- Acquisition and data management of analog and discrete inputs, including inputs from NERVIA networks
- Execution of the application software
- Transmission of output data to analog and discrete outputs, including outputs to NERVIA networks

The critical characteristics for acceptance were verified as specified in the following test procedures:

- System Setup and Checkout Test Procedure (3 010 294 B), which was submitted to NRC by Rolls-Royce letter dated June 15, 2010
  - Attachment 4, Normal Operating Performance Data Verification Checklist
- Environmental Test Procedure (3 010 287 B), which was submitted to NRC by Rolls-Royce letter dated June 15, 2010
  - Attachment 3, Normal Operating Performance Data Verification Checklist
  - Attachment 4, Data Evaluation For Normal Operating Performance
- Seismic Test Procedure (3 010 288 B), which was submitted to NRC by Rolls-Royce letter dated June 15, 2010
  - Attachment 3, Data Evaluation For Normal Operating Performance
  - Attachment 4, Normal Operating Performance Data Verification Checklist
- EMI/RFI Test Procedure (3 010 289 A), which was submitted to NRC by Rolls-Royce letter dated March 31, 2011
  - Attachment 4, Data Evaluation For Normal Operating Performance
  - Attachment 5, Normal Operating Performance Data Verification Checklist
- Electrostatic Discharge (ESD) Test Procedure (3 010 292), which was A submitted to NRC by Rolls-Royce letter dated March 31, 2011
  - Attachment 3, Data Evaluation For Normal Operating Performance
  - Attachment 4, Normal Operating Performance Data Verification Checklist
- Electrical Fast Transient (EFT) Test Procedure (3 010 290 B), which was submitted to NRC by Rolls-Royce letter dated March 31, 2011
  - Attachment 3, Data Evaluation For Normal Operating Performance

  - Attachment 4, Normal Operating Performance Data Verification Checklist
- Surge Withstand Test Procedure (3 010 291 A), which was submitted to NRC by Rolls-Royce letter dated March 31, 2011
  - Attachment 3, Data Evaluation For Normal Operating Performance
  - Attachment 4, Normal Operating Performance Data Verification Checklist
- Operability Test Procedure (3 010 295 B), which was submitted to NRC by Rolls-Royce letter dated June 15, 2010
  - Section 7- Failover Operability Test
    - Attachment 3, Normal Operating Performance Data Verification Checklist
  - Section 8 - Loss Of Power Test
    - Attachment 3, Normal Operating Performance Data Verification Checklist
    - Attachment 4, Data Verification Checklist After System Reset
    - Attachment 5, Resume Normal Operation Data Verification Checklist
    - Attachment 6, Loss Of Power Data Verification Checklist
    - Attachment 7, System Reset Data Verification Checklist
  - Section 9 - Power Interruption Test
    - Attachment 3, Normal Operating Performance Data Verification Checklist
  - Section 10 - Power Quality Tolerance Test
    - Attachment 3, Normal Operation Data Verification Checklist
    - Attachment 4, Normal Operation Data Verification Checklist
    - Attachment 5, Normal Operation Data Verification Checklist
    - Attachment 6, Normal Operation Data Verification Checklist

The following documents exist (and have been submitted to NRC) that describe the ***SPINLINE 3*** qualification testing:

- Equipment Qualification Plan (3 006 501 D)
- System Setup and Checkout Test Procedure (3 010 294 B)
- Radiation Exposure Test Procedure (3 010 286 B)
- Environmental Test Procedure (3 010 287 B)
- Seismic Test Procedure (3 010 288 B)
- EMI / RFI Test Procedure (3 010 289 A)
- ESD Test Procedure (3 010 292 A)
- Electrical Fast Transient Test Procedure (3 010 290 B)
- Surge Withstand Test Procedure (3 010 291 A)
- Class 1E to Non-Class 1E Isolation Test Procedure (3 010 293 A)
- System Setup and Checkout Test Procedure (3 010 294 B)
- Operability Test Procedure (3 010 295 B)
- Prudency Test Procedure (3 010 296 B)

The results of the qualification testing will be documented in a various text reports described in the Equipment Qualification Plan.

All of these documents are maintained in the Rolls-Royce records management system.

A compliance matrix showing the alignment of the ***SPINLINE 3*** qualification program to the generic requirements in EPRI TR-107330 Sections 5 and 6 will be provided by February 28, 2012. This document will also include a matrix of the critical characteristics for acceptance and the methods used by Rolls-Royce for acceptance.

Rolls-Royce Answer to Part b) item ii - Method 2 was applied to the ***SPINLINE 3*** technology in three broad parts. First, the ***SPINLINE 3*** software development process (based on International Electrotechnical Commission standard IEC 880-1986) was compared to the applicable NRC review guidance for safety system software development defined in NRC Branch Technical Position 7-14. Second, the ***SPINLINE 3*** development process was compared to the applicable US industry process standards applied to software development for safety systems. And third, the ***SPINLINE 3*** platform design characteristics were compared to the applicable US regulatory guidance.

As noted in EPRI NP-5652 Section 3.2.3 states that "Two basic criteria must be met when conducting a commercial grade survey. The purchaser must confirm that the selected commercial grade item's critical characteristics are controlled under the scope of commercial quality system activities. The purchaser must also be reasonably assured that the commercial supplier's activities adequately control the commercial grade items supplied."

The results of the comparison of the ***SPINLINE 3*** software development process to Branch Technical Position 7-14 are documented in the following tables in LTR Appendix A:

- Table 3.10-1, IEC 880-1986 Appendix B Compliance Matrix
- Table 3.10-2, Comparison of IEC 880-1986 and NRC Branch Technical Position 7-14 Requirements

The results of the comparison of the ***SPINLINE 3*** development process to the applicable US industry process standards applied to hardware and software development for safety systems are documented in the following tables in LTR Appendix A:

- Table 3.1-1, Standard Review Plan Table 7-1 Compliance Summary
- Table 3.2-1, 10CFR50 Appendix B and ASME NQA-1-1994 Map to Corresponding I&C France QA Plans & Procedures
- Table 3.2-2, 10CFR50 Appendix B and ASME NQA-1-1994 Map to Corresponding I&C US QA Plans & Procedures
- Table 3.8-1, IEEE 7-4.3.2-2003 Compliance Matrix
- Table 3.8-3, Mapping ***SPINLINE 3*** SQP MC3 and Other Content to IEEE 730-1998 SQAP Content Guidance
- Table 3.8-4, Mapping ***SPINLINE 3*** SMQP and Other Content to IEEE 730-1998 SQAP Content Guidance
- Table 3.8-5, Mapping ***SPINLINE 3*** Application SQAP and Other Content to IEEE 730-1998 SQAP Content Guidance
- Table 3.8-6, Mapping ***SPINLINE 3*** SQP MC3 and Other Content to IEEE 828-1998 SCMP Content Guidance
- Table 3.8-7, Mapping ***SPINLINE 3*** Platform SCMP and Other Content to IEEE 828-1998 SCMP Content Guidance
- Table 3.8-8, Mapping ***SPINLINE 3*** Application SCMP and Other Content to IEEE 828-1998 SCMP Content Guidance
- Table 3.8-9, Mapping ***SPINLINE 3*** SQP MC3 and Other Content to IEEE 1012-1998 SVVP Content Guidance
- Table 3.8-10, Mapping ***SPINLINE 3*** SMQP and Other Content to IEEE 1012-1998 SVVP Content Guidance

- Table 3.8-11, Mapping ***SPINLINE 3*** Application SVVP and Other Content to IEEE 1012-1998 SVVP Content Guidance
- Table 3.8-12, Alignment of IEEE 1074-1995 Activities, ISG-06 Tier 3 Document Guidance, and ***SPINLINE 3*** Documents

These comparisons demonstrate that the Rolls-Royce processes used for ***SPINLINE 3*** software development provided adequately control of the software development."

The ***SPINLINE 3*** development process comparison is supplemented with the information provided in Rolls-Royce document Map of ISG-06 Tier 3 Submittal Guidance to Generic ***SPINLINE 3*** Digital Safety I&C Platform Licensing Documents (3 011 552) provided to NRC by Roll-Royce letter dated March 31, 2011.

The results of the comparison of the ***SPINLINE 3*** platform design characteristics to the applicable US regulatory guidance are documented in the following tables in LTR Appendix A:

- Table 3.6-1, Responses to NUREG/CR-6082 Communications System Questions
- Table 3.7-1, Interim Staff Guide DI&C-ISG-04 Compliance Matrix
- Table 3.8-2, IEEE 603-1991 Compliance Matrix

These results demonstrate that the ***SPINLINE 3*** system developed with the Rolls-Royce processes meets the identified critical system characteristics.

The ***SPINLINE 3*** digital safety I&C platform has the following general attributes:

- Fail-safe: ***SPINLINE 3*** assures that, in case of detected failure, the outputs associated with a central processing Unit achieve a pre-defined safe position.
- Fault-tolerance: ***SPINLINE 3*** supports system architectures that meet the redundancy requirements of the single failure criterion. In addition, ***SPINLINE 3*** microprocessors can automatically reconfigure their voting logic to accomplish the intended safety function with one or more divisions out of service.
- Diversity: ***SPINLINE 3*** supports system architectures that employ signal diversity to defend against common cause failures. ***SPINLINE 3*** also can be deployed as a diverse system as part of a plant-level defense-in-depth and diversity strategy.
- Functional isolation: ***SPINLINE 3*** equipment and communications design prevents propagation of failures between,redundant equipment in separate divisions. In addition, communication paths to nonsafety I&C systems are electrically isolated with one-way communications from ***SPINLINE 3*** to the nonsafety I&C system. This prevents faults in a non-safety I&C system from affecting ***SPINLINE 3***.
- Determinism: For all processing, the same inputs produce the same outputs within a guaranteed response time.
- Ease of use: Operation and maintenance are simplified by automated on-line system supervision, fault detection, and self-diagnosis.
- Flexibility: Through carefully controlled processes, many system operating characteristics can be updated without hardware modification.
- Modularity: ***SPINLINE 3*** can be delivered either in standard chassis to be integrated into existing cabinets (for refurbishment purposes) or in new cabinets.
- Scalability: ***SPINLINE 3*** has been deployed internationally in a wide variety of safety I&C applications, including Reactor Trip System, Engineered Safety Feature Actuation System, Nuclear Instrumentation System, and diverse trip system applications.

- Secure development and operational environment: The software life cycle processes applied by Rolls-Royce establish a secure development and operational environment for managing the generic ***SPINLINE 3*** platform baseline and developing the plant-specific application software through the factory test phase. These processes protect against unauthorized, unintended, and unsafe modifications to the system, and support implementation of design requirements that promote integrity and reliability during operation and maintenance in the event of inadvertent operator actions or undesirable behavior of connected equipment

Twelve generic board-level Reliability and Predictive Safety Analysis reports were prepared to assess the failure modes and effects of the individual modules and provide reliability estimates for each board. These analyses were submitted to NRC by Rolls-Royce letter dated December 23, 2009. The reliability assessments for the ***SPINLINE 3*** hardware were summarized LTR Section 5.2. These reliability characteristics represent Method 2 dependability characteristics for acceptance.

The ***SPINLINE 3*** OSS originally was designed and validated based on the requirements provided in IEC 880-1986, which provides technical and process requirements for the development of software in the safety systems of nuclear power plants. These requirements include the following:

- no interrupts
- no dynamic memory allocation
- no support for event driven multi-tasking
- be simple and include only the functions and components necessary for I&C safety functions
- be self-tested
- include defense-in-depth safety programming
- execution must be safety oriented (i.e., go to a safe position when a failure is detected)

These requirements represent critical design performance characteristics that were verified and/or validated during the development process described in ***SPINLINE 3*** LTR Section 6.2. Of particular interest to NRC is the validation testing of the ***SPINLINE 3*** OSS. This testing was performed as part of the original software development. As such, it was assessed as part of the Method 2 effort. The critical dependability characteristics for acceptance include the following validation test documents:

- ***SPINLINE 3*** Technical Instruction V&V of software components (1 207 107D) - This technical instruction sets the verification and validation rules for safety-classified software components. This document was submitted to NRC by Rolls-Royce letter dated December 23, 2010.

- ***SPINLINE 3*** Safety of Processing Unit Software (1 207 228 H) – Section 2.5 describes the overall Test strategy for the ***SPINLINE 3*** OSS. The tests performed on the Class 1E OSS are:
  - Unit tests of each module, The unit tests are comprised of [[

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- Integration tests - The purpose of integration tests is to ensure that mutual relations between software modules and relations between these modules and the target hardware are in accordance with the design.
- Validation tests - The purpose of validation tests is to check that the software operates in accordance with the specification.

This document was submitted to NRC by Rolls-Royce letter dated December 23, 2009.

- ***SPINLINE 3*** / OSS / Software Validation Test Plan (1 207 146 G) - This document constitutes the OSS Validation Tests Analysis for safety class Units. This software is applicable to software developments for 1E-class Units which based on ***SPINLINE 3***-standard boards and are compatible with ***SPINLINE 3*** technology. It defines the strategy employed in the tests performed in order to check that the OSS operates in accordance with specified requirements. The document covers all of the functions indicated in the OSS System Requirements Specification (1 207 108 J) for safety class Units. Validation tests are defined in a [[

]] The critical design performance characteristics validated in the original development process are identified in Section 5 of this document. This document was submitted to NRC by Rolls-Royce letter dated February 1, 2010.

- ***SPINLINE 3*** / OSS / Software Validation Test Report (1 207 232 F) - This document contains the following information:
  - Section 2 provides information of the environment required for the execution of the tests, indicating the hardware, software, and test sets used.
  - Section 3 describes the layout and content of the test forms and test reports.
  - Section 4 contains all of the test forms corresponding to the tests identified in the Software Validation Test Plan (1 207 146 G). Each form sets out the test procedure together with the expected results of the tests. This section contains all of the test forms designed for this software, even including those which were not used in the most recent test run.
  - Section 5 contains the test run reports for each version of the software,
  - The appendices contain all non-conformity reports for each version of the software.

This document was submitted to NRC by Rolls-Royce letter dated February 1, 2010.

- ***SPINLINE 3*** / CSS / Software Integration Test Plan and Report (1 207 204 E) - This document contains the following information:
  - Section 2 outlines:
    - the test strategy,
    - the various stages of the integration process and the order in which these steps are performed.
  - Section 3 describes the test facilities required for the integration of the Core System Software (CSS), i.e.:
    - hardware requirements,
    - software requirements,
    - test configurations.
  - Section 4 describes implementation of the tests. This section includes:
    - a description of the test forms and test reports,
    - all procedures for tests and associated verifications. These procedures are referred to later in the test description (test forms).
  - Section 5 gives a detailed description of the tests to be performed at each stage of the integration process.
  - Section 6 relates to test coverage, i.e. the relationship between the modules and the tests for the various steps in the integration process.
  - Section 7 sets out the principles applied to determine which tests need to be run again if the software is upgraded (i.e. tests associated with the upgrade and regression tests).
  - Section 8 contains reports on the different tests performed and includes the following information for each version of the CSS:
    - description of characteristics for the various test sequences performed,
    - a table summarizing data for the test sequences performed,
    - conclusions arising from the test sequences performed.
  - Section 9 provides an index for the different test cases identified in section 2 and for the various test procedures and verifications specified in section 3.
  - Section 10 at the end of the document contains the appendices. There is an appendix for each version of the CSS, containing nonconformance reports covering the non-conformities detected during the different test sequences.

  This document was submitted to NRC by Rolls-Royce letter dated February 1, 2010.

These results demonstrate that the ***SPINLINE 3*** software was appropriately tested with a rigorous validation process, that high quality test documentation was available to describe the testing performed and results obtained, and that the test results remain valid through the implementation of the Rolls-Royce design control and configuration management systems.

The assessment of the ***SPINLINE 3*** platform development process described in ***SPINLINE 3*** LTR Section 6.3 and Appendix A as well as Rolls-Royce document Map of ISG-06 represents the Method 2 data. These development process characteristics represent Method 2 dependability characteristics for acceptance. The ***SPINLINE 3*** Design Analysis Report (MPR Document No. MPR-3337, Revision 1) provides an independent assessment of documented evidence related to the ***SPINLINE 3*** platform software design and software life cycle processes and determine if there is an adequate technical basis for dedication of the platform software using the process defined in EPRI technical reports TR-107330 and TR-106439. MPR's favorable conclusions are documented in the report. The MPR work builds on previous assessment work they had performed with EPRI on the ***SPINLINE 3*** technology. The MPR Design Analysis Report was submitted to NRC by Rolls-Royce letter dated July 1, 2009.

All of these documents cited in the Tables in LTR Appendix A and Rolls-Royce document Map of ISG-06 are maintained in the Rolls-Royce records management system.

A compliance matrix showing the alignment of the ***SPINLINE 3*** qualification program to the generic requirements in EPRI TR-107330 Sections 4 and 7 will be provided by February 28, 2012. This document will also include a matrix of the critical characteristics for acceptance and the methods used by Rolls-Royce for acceptance.

The use of Method 2 is appropriate to accept the original development test records, since the review for acceptance was done during the dedication period and the review was performed with a program in accordance with 10 CFR Part 50 Appendix B requirements whereas the original validation test was not.

The results of the Method 2 review of the validation testing were favorable. The review found that the development processes (including the original validation testing) were rigor and comparable to US nuclear safety standards, the development documentation was available and of high quality, and the design and test results remain valid.

EPRI TR-106439 envisioned the approach of using the historical development records as a basis for acceptance in a commercial grade dedication review.

EPRI TR-106439 notes on page 3-3 in the discussion on the equivalent assurance for commercial equipment that "Because the vendor does not have a 10 CFR 50 Appendix B quality assurance program, the process that was followed in development and verification of the product may not have included all of the elements of an Appendix B program, and documentation of the process may be lacking." The Rolls-Royce review of the ***SPINLINE 3*** software development process found that it was comparable to an Appendix B program and that the full set of development documentation was available.

EPRI TR-106439 notes on page 3-4 that:

> Additional activities will be required by the dedicator to reach an adequate level of assurance for a commercial grade item. An example would be additional testing needed to supplement the vendor's tests and build confidence in the device and its functionality, or to examine its response to specific conditions or abnormal events. Additional reviews or analyses may be needed (e.g., review of the device design and analysis of its failure modes), depending on the extent of reviews and verifications performed by the vendor during product development. Additional documentation may need to be produced, for example, in areas where it is evident that some process steps were performed by the vendor but not adequately documented.

The Rolls-Royce review of the ***SPINLINE 3*** platform development process found that additional hardware qualification testing was needed to demonstrate performance in to response the specific conditions or abnormal events outlined in the EPRI TR-107330 regimen of Operability and Prudency tests. On the other hand, Rolls-Royce found that no additional activities were required to supplement the original software development process or validation testing.

EPRI TR-106439 notes on page 4-5 in the discussion on performance characteristics that:

> These include the functionality required of the device (the "must-do" functions) and performance related to this functionality (e.g., response time). They also include environmental requirements related to the needed performance (e.g., meeting accuracy requirements over a specified range of ambient temperatures). The acceptance criteria and verification methods for these again are similar to those for analog equipment. However, this category also includes characteristics related to failure management and "must-not-do" functions. For example, based on a failure analysis the utility may require specific behavior of the device under certain abnormal or faulted conditions. Acceptance criteria might include items such as detection of classes of failures, and "preferred" or fail-safe failure modes to be entered under prescribed circumstances (e.g., a specific output state required on loss of power or signal input). Verification methods include testing and design reviews, supported by failure analysis and reviews of operating history. These activities can involve Methods 1 (Tests and Inspections), 2 (Commercial Grade Survey), and 4 (Supplier/Item Performance Record) of EPRI NP-5652.

The Rolls-Royce review of the ***SPINLINE 3*** platform development process found that additional hardware qualification testing was needed to demonstrate performance in to response the performance and failure management conditions outlined in EPRI TR-107330 regimen of Operability and Prudency tests. On the other hand, Rolls-Royce found that no additional activities were required to supplement the original software development process or validation testing.

EPRI TR-106439 notes in Table 4-1 on the discussion of performance characteristics that:

> The dedicator typically reviews tests that were performed by the vendor or a third party, and runs supplementary tests as part of the dedication. Some characteristics may be verified through special stress or "challenge" testing performed by the vendor or dedicator (e.g., tests of performance under conditions of

The Rolls-Royce review of the ***SPINLINE 3*** platform development process found that additional hardware qualification testing was needed to demonstrate performance in to response the challenge testing outlined in EPRI TR-107330 regimen of Operability and Prudency tests. On the other hand, Rolls-Royce found that no additional activities were required to supplement the original software development process or validation testing.

EPRI TR-106439 Table 4-2 provides an example on the assessment of "built-in quality" for commercial digital equipment that addresses the review of vendor testing:

Review of vendor testing	Functional and performance testing Environmental testing including EMI/RFI Extent of software verification testing (e.g., module, line, or branch coverage) Extent of validation testing (e.g., static, dynamic, random) Extent of challenge testing (e.g., tests specifically designed to uncover failure modes) Documentation of testing

The Rolls-Royce review of the ***SPINLINE 3*** platform development process found that additional hardware qualification testing was needed to demonstrate qualification to environmental, seismic and EMI/RFI conditions and in to response the challenge testing outlined in EPRI TR-107330 regimen of Operability and Prudency tests. On the other hand, Rolls-Royce found that no additional activities were required to supplement the original software development process or validation testing. The validation tests were found to be comprehensive with regard to functional, performance, and fault management requirements.

The results of the commercial grade dedication effort for software and firmware installed on various I/O modules is discussed in the response to RAI-5.

Rolls-Royce Answer to Part b) item iii - Rolls-Royce has been designing and manufacturing safety I&C systems for nuclear power plants for more than 30 years. Rolls-Royce originally developed non-software-based analog safety I&C systems for the Électricité de France (EDF) fleet of 900 megawatt pressurized water reactors (PWRs). In the 1980s, Rolls-Royce designed and deployed two generations of software-based digital safety I&C systems for EDF's later fleet of P4 and N4 PWRs. ***SPINLINE 3*** is the next generation of Rolls-Royce digital safety I&C systems. This chapter provides an overview of ***SPINLINE 3*** development and operational use in the many French and international nuclear power plants where it is currently deployed in a variety of digital safety I&C applications. This historical information is intended to illustrate the substantial legacy of safety I&C developments that led to the ***SPINLINE 3*** digital safety I&C platform, which is the subject of this LTR.

The evolution of the ***SPINLINE*** is shown in Figure Q11-1. The operating experience summarized in ***SPINLINE 3*** LTR Section 2 and section 6.1 correlates to the Method 4 data that demonstrates that the ***SPINLINE 3*** technology has operated reliably in typical nuclear power plant environments.

EPRI TR-106349 and EPRI TR-107330 discuss the use of operating experience in support of the commercial grade dedication of a legacy digital system. In particular, operating experience can be used in the following ways:

- If the device has been applied previously (it is not the first of its kind), its operating experience may be reviewed to determine whether it has been satisfactory.
- The qualifier may compensate for shortcomings in legacy software by evaluating documented operating experience in applications similar to nuclear safety related applications, and by performing tests of legacy software to confirm conformance to requirements.
- If operating experience is used as a basis for establishing module failure rates, the PLC manufacturer must have a problem reporting and tracking program.

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From the beginning, Rolls-Royce hardware components and systems were designed, implemented, and qualified in compliance with European nuclear standards, including the International Atomic Energy Agency (IAEA) 50-C-QA code for quality assurance and the French national code RCC-E, which prescribes requirements for qualification of electrical equipment used in French-built nuclear power plants. This experience provided a strong foundation in nuclear safety system design requirements that provide the basis for the modular nature of the ***SPINLINE 3*** technology that provides the flexibility to meet customer performance requirement (e.g., functionality and reliability) and local regulatory requirements (e.g., redundancy, independence, and diversity).

The Rolls-Royce safety software evolved in stages to adapt to the introduction of new digital components and software methods and tools. These evolutionary stages started with software development "from scratch" using low-level manual coding and have now matured into processes based on high-level languages, including application-oriented languages, code re-use and automated code generation.

The P4 SPIN software was developed using life cycle processes targeted to produce "close to zero faults" software. The main features are:

- A "V" model software development cycle
- A top-down modular design
- Design and coding rules aimed at developing reliable software
- A Verification and Validation (V&V) team independent of the software design team
- The verification of all design documents and source code
- "White box" unit testing of all the software modules, achieving 100% branch coverage
- "Black box" validation testing performed at the processing unit level, channel/division/train level, and system level

This technology uses the Motorola 6800 microprocessor with unidirectional and asynchronous communication links for data exchange. A single P4 unit's SPIN system has 52 safety processing units distributed in a four-channel architecture. Today, 20 P4 SPIN systems are in operation with a total of 1,040 safety processing units. P4 SPIN systems have accumulated more than 500 reactor-years of operation.

The P4 SPIN software consists of about 40,000 instructions written in 6800 assembly code. This software includes the application software performing the processing of the safety functions, and the OSS that performs data acquisition, actuator control, data communication, and hardware self-supervision functions.

This main software development effort took place during the years 1981 and 1982 and was performed according to the guidance in working drafts of the future IEC 880 standard, which was intended to significantly improve the reliability of software used for the implementing nuclear safety functions. The feedback of experience gained on the P4 project was a major input to this IEC 880 standard which was eventually issued in 1986. This experience provided a strong foundation in nuclear safety system software development.

The EDF N4 project deployed 1450 megawatt four-loop PWRs with a fully-computerized Main Control Room that implemented new I&C technologies. For the N4 nuclear power plants, Rolls-Royce developed a new generation of its software-based safety I&C system technology, called N4 SPIN, which is based on the Motorola (now Freescale) MC68000 family of microprocessors and on an Rolls-Royce proprietary high-speed deterministic communications network called NERVIA. The main improvements relative to the P4 SPIN technology were:

- A reduction in the number of separate functional processing units, from seven for P4 to five for N4, enabled by the greater processing power of the 68000 microprocessor;
- The NERVIA digital communications network, which allowed for a significant reduction of electronic boards and wiring; and
- The implementation of software-based voting units for both the Reactor Protection System and the Engineered Safety Feature Actuation System actuators.

A single N4 unit's SPIN system uses 40 safety processing units used in a four channel / two output train system architecture. Today, four N4 SPIN systems are in operation with a total of 160 safety processing units. The same digital safety I&C technology is also employed in the protection systems of 11 research reactors. The N4 SPIN has been in operational use since the first N4 plant commissioning tests in 1991 and has been in commercial operation since 1996. N4 SPIN systems have accumulated more than 50 reactor-years of operation.

The N4 SPIN software consists of about 200,000 instructions implemented in C language, most of them generated from 200 graphical views created using a proprietary Functional Block Diagram language named SAGA.

As for the P4 project, the N4 software was developed with the objective of producing "close to zero faults" software, using basically the same software life cycle processes, but with intensive use of software tools for the tasks that could be automated or assisted.

This main software development effort for the N4 project took place during the years 1988 and 1989 and was performed according to the guidance provided in IEC 880-1986. The basic processes for developing the N4 safety software have not changed since the P4 project. However, process changes were made to take into account the evolution in languages and tools used for the N4 project and evolution in software engineering processes not explicitly required in IEC 880-1986, such as requirements for dedicated software plans.

The ***SPINLINE 3*** platform was developed between 1993 and 1996, based on the N4 technology. It includes enhancements to the N4 hardware and the development of platform software and tools needed to produce an adaptable safety I&C platform suitable for use worldwide in refurbishment of existing nuclear power plant safety I&C systems and for new construction safety I&C systems. The main improvements relative to the N4 SPIN technology are:

- Hardware:
  - New EMC-proofed chassis, cabling, and terminal blocks
  - Additional CPU, (I/O), and communication boards
- Software:
  - Configurable OSS,
  - An enhanced software engineering tool set, including a platform-dedicated tool to configure and set the parameters for the processing Units and NERVIA networks
  - A non-proprietary version of the SAGA environment called the Safety Critical Application Development Environment (SCADE), developed and maintained by the software company Esterel Technologies.

The software for the ***SPINLINE 3*** platform also builds on N4 software design and experience. The following software was developed for the ***SPINLINE 3*** platform:

- A Class 1E standardized OSS, which creates the environment in which the ***SPINLINE 3*** application software runs
- A Class 1E application-oriented library of re-usable software components
- Class 1E software embedded in the communication board of the 10 megabits/second version of the NERVIA network
- A non-Class 1E set of tools integrated in a software development environment called CLARISSE, which is used for the configuration of the OSS and for the development of the application software for ***SPINLINE 3*** systems

SPINLINE 3 has been implemented successfully for the refurbishment of Class 1E I&C systems on several models of PWR nuclear power plants and on several Russian-designed nuclear power plants, including both VVER and RBMK. ***SPINLINE 3*** also is deployed in safety I&C systems on several new PWRs in the Republic of China. ***SPINLINE 3*** systems have accumulated more than 220 reactor-years of operation.

The life cycle processes for the ***SPINLINE 3*** platform software were established according to the guidance provided in IEC 880-1986 and were documented in dedicated software plans. The ***SPINLINE 3*** software life cycle processes also took into account additional process enhancements employed on the N4 project and ongoing standardization works for a supplement to IEC 880, which was issued in 2000. The experience gained at Rolls-Royce in developing several safety I&C systems using the ***SPINLINE 3*** digital I&C platform was an input to the revision of IEC 880-1986, which started in 2001 and was completed in 2006 as IEC 60880 Edition 2. The project leader for this revision was from Rolls-Royce.

The generic ***SPINLINE 3*** platform now is managed under a quality assurance program that complies with 10 CFR Part 50 Appendix B.

The base of ***SPINLINE*** nuclear operating experience to validate performance that has provided opportunities to identify latent errors. As a consequence of the high quality software development, the feedback of experience gained from the P4, the N4, and the ***SPINLINE 3*** safety I&C systems is that no failure with software as a root cause has been detected during operation in installed Class 1E systems. In addition, operating experience with ***SPINLINE 3*** systems and the previous generations of Rolls-Royce digital safety I&C systems has shown no instances where the capability of the safety I&C system to perform its intended safety function(s) was compromised during an anticipated operational occurrence. Specifically, the ***SPINLINE 3*** systems have not experienced an unsafe condition in more than 199 reactor-years of operation as of December 2011.

Rolls-Royce has a problem reporting and tracking system as described in the Rolls-Royce Civil Nuclear SAS Instrumentation & Control Quality Manual (8 303 186 P), which was submitted to NRC by Rolls-Royce letter dated July 1, 2009. The applicable implementing procedures are identified in ***SPINLINE 3*** LTR Table 3.2-1 Item XV – Nonconforming Materials, Parts of Components and Item XVI – Corrective Action).

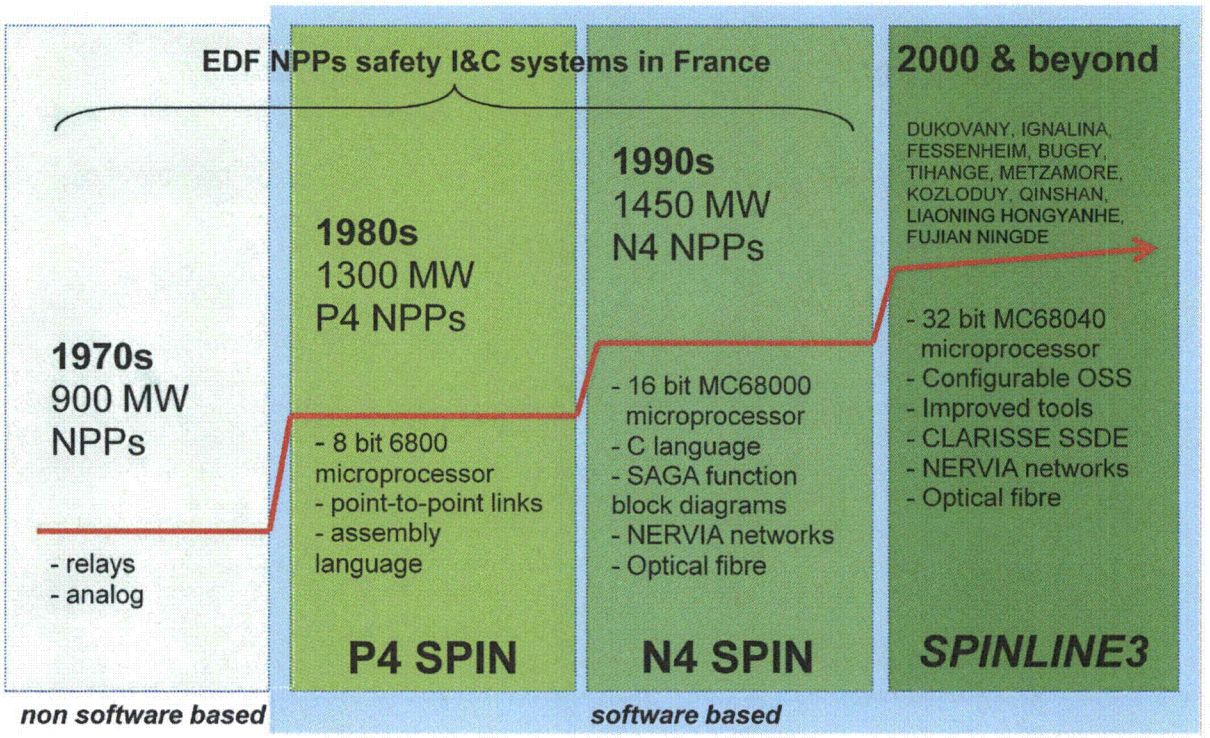

Figure Q11-1: Evolution of the ***SPINLINE 3*** Product Line

RAI-12: Clarify the following:

a. The referenced design document is entitled "Software Preliminary Design." Clarify whether this is an artifact of when the document was originally released, or whether there is a "Final" design document.
b. The software requirements specification referenced appears to be a design description document rather than a requirements specification. Clarify whether there is another software requirements specification (i.e., one that would contain the actual system requirements – "shall" or "will" statements – that are verified).
c. The RRCN CGD plan and report both identify RRCN 3 010 612 A as the MCL that is relied upon for identifying product and part numbers relative to critical physical characteristics for the system. However, RRCN 3 010 612 D is the version on the docket (not 3 010 612 A). Clarify whether "D" is an updated version of "A" and whether "D" is the correct revision to review.
d. In the software requirements specification and software preliminary design documents reference is made to the "Workshop." Describe what the "Workshop" is in the context of SPINLINE 3.
e. The CGD plan and report both reference Appendix A of the LTR as containing the equipment data sheets; however, this information appears to be in Appendix B. Please clarify if Appendix B is the correct reference.

Rolls-Royce Answer to Part a) - The "Software Preliminary Design" should not be considered as an "artifact"; instead, it is a "final high level" description introducing the detailed design. The aim of the preliminary design phase is to define the software architecture. The aim of the detailed design phase is to use the results of the preliminary design to obtain a sufficient level of detail with regard to both algorithms and data structure to proceed with coding. The Software Preliminary Design document is a final design document which describes the architecture of the software, the main modules, and their interfaces. The software development document hierarchy is shown in ***SPINLINE 3*** LTR Figure 6.2-1 and described in Section 6.2.2.2. The detailed design documents are described in Section 6.2.2.3.

Rolls-Royce Answer to Part b) - Rolls-Royce does not use rules for expressing the requirement as it is common for "standards" ("shall" and "should" or sometimes "may"). The documents are written as the description of what the software is to do (i.e., they do express the software requirements). There is no other software requirements specification.

Rolls-Royce Answer to Part c) - The letter designation reflects the revision level for a document. As such, revision D is a later version of the document than revision A. Revision A of 3 010 612 was in effect when the commercial grade dedication plan was issued. The dedication effort related to plan item 4.2.1A (product / part identification) was done examining revision D. It was the current revision of the document when the dedication task was completed in February 2011.

In revision A the configuration part identification information was not included. It was noted with the following sentence: "This section will be filled in a later revision of the MCL". The part numbers were added in revision B. The part numbers themselves did not change in subsequent revisions. The differences in later versions are related to the revision levels associated with part numbers and document identifiers. For example, the only change of part number revision between document revisions C and D) was for the Data Acquisition System (part number ANC00000023 revision C to D) used for the qualification testing program. Revision changes on part numbers are performed and tracked according to the "change management process (8 303 197).

Rolls-Royce Answer to Part d) - The Software Preliminary Design (1 207 141 H) defines Workshop as the software engineering workshop, called "CLARISSE" in Section 1.2. The Software Requirements Specification (1 207 108 J) describes the CLARISSE workshop in Section 2.1.1. The CLARISSE tool is also described in ***SPINLINE 3*** LTR Section 4.4.4.4 as the System and Software Development Environment.

Rolls-Royce Answer to Part e) - The compliance tables moved from Chapter 3 to Appendix A and the equipment datasheets moved to Appendix B in Revision C of the ***SPINLINE 3*** LTR. The Commercial Grade Dedication Plan was issued prior to Revision C. The Commercial Grade Dedication Report should have referred to Appendix B.

Environmental Qualification

The following RAIs address regulatory evaluation criteria for the environmental test conditions that apply to safety-related equipment qualification (EQ) for use in a mild environment. Regulatory Guide (RG) 1.209 (ADAMS Accession No. ML070190294), Regulatory Position 1, provides applicable guidance. RG 1.209 endorses Institute of Electrical and Electronics Engineers Standard 323-2003. Section D.5.4.1 of Digital I&C-ISG-06 provides additional guidance.

RAI-13: Section D.8 of the Environmental Test Plan, included in the EQ Plan (3 006 501 D) states that the low temperature and low humidity tests would be performed separately due to limitations in the test chamber. Describe how the combination of these environmental conditions sufficiently envelope the SPINLINE 3 Platform's susceptibility to synergistic effects for these service conditions.

Rolls-Royce Answer - The testing in NTS laboratory was performed as described in the Environmental Test Procedure 3010287 C, and according to Note 1 of EPRI TR-107330 Figure 4-4. The test was run for 8 hours at 35°F and 12% humidity. Another test was run at 5% humidity at 77°F. Operability testing was performed between the two tests and after both tests were run. The test execution was recorded in the completed test procedure (document to be issued).

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]] As noted in Regulatory Guide 1.209:

> IEEE revised the industry guidance for qualification, IEEE Std. 323, in 2003. A particular distinction between IEEE Std. 323-2003, "IEEE Standard for Qualifying Class 1E Equipment for Nuclear Power Generating Stations" (Ref. 7), and IEEE Std. 323-1974 (Ref. 5), is that the current version does not require age conditioning to an end-of-installed-life condition for equipment in mild environments where significant aging mechanisms are not present."

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The Rolls-Royce assessment is consistent with the conclusions in the NRC safety evaluation report for EPRI TR-107330, which accepted the test guidance contained in Note 1 of EPRI TR-107330 Figure 4-4. The test was run for 8 hours at 35°F and the lowest relative humidity and then another test was run at 5% humidity and lowest temperature, not exceeding 140°F. The note allows the low temperature low humidity test conditions to be decoupled, as necessary based on the test chamber capabilities. The high temperature high humidity test conditional cannot be decoupled. The basis for the NRC conclusion on environmental testing is not documented in the safety evaluation report; however, it is likely that they were based on the NRC-sponsored research being conducted in the same time period. NUREG/CR-6479, Technical Basis for Environmental Qualification of Microprocessor-Based Safety-Related Equipment in Nuclear Power Plants, issued in December 1997 contains a conclusion from the work done by Oak Ridge National Laboratory on environmental stressor effects testing. The report noted that with "regard to temperature and humidity, the study found that the combination of high temperature at high relative humidity was the condition to affect the Experimental Digital Safety Channel, rather than temperature acting alone.

RAI-14: The SPINLINE 3 "Qualification Test Specimen and Test System with System Specification for the Qualification Test Specimen and Data Acquisition System" (3 006 404 E) does not define the cycle time for the Test Specimen Application Program (TSAP) running in the SPINLINE 3 Qualification Test Specimen (QTS). Section 4.4.3.2 of the LTR states that the CPU runs under a fixed cycle time, making the system run in a cyclical mode. Please describe the CPU cycle time and processing load during EQ testing. Also, please describe if the system performance, such as cycle time and processing load, can be affected by changes in environmental conditions.

Rolls-Royce Answer – The QTS cycle time of 20 milliseconds is defined at several points in System Specification 3 006 404 E. [[

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RAI-15: Section 5.4 of the LTR states that a different relay output circuit would be used during seismic testing. Please clarify that the relay output circuit would be modified for seismic test to detect chattering during application of the operating basis earthquakes and safe shutdown earthquake vibrations.

Rolls-Royce Answer - The basic relay output circuits implemented on the QTS are used to monitor the relays, using only two DAS inputs. The basic circuit is used for most of the QTS relays. During seismic testing, relays and related contacts should be fully monitored to check for chattering. In order to fully monitor all the relay contacts during seismic testing, another circuit is implemented, which consumes many more DAS inputs. The fully monitored circuit is implemented on a subset of relays.

Any of these circuits (as shown in System Specification Figures 11 and 12) may be implemented in application systems.

Rewording of the System Specification, section 5.4 (last sentence on page 52) will be as follows:

> During seismic testing, relays and related contacts should be fully monitored to check for chattering. For that reason, a different relay output circuit (shown in Figure 12) will be used on some relays. This circuit provides for indication for all inadvertent contact failure. The basic circuits (figure 11) are implemented on all other relays.

RAI-16: RRCN is using guidance provided in EPRI TR-107330 for generically qualifying the SPINLINE 3 platform. However, RRCN did not prepare a compliance traceability matrix with this EPRI document. Instead, RRCN prepared LTR Table 5.1-1, *Generic Qualification Envelope for the SPINLINE 3 Digital Safety I&C Platform*, to provide comparable information. Table 5.1-1 defines test levels and acceptance criteria for the generic qualification envelope. Please clarify whether RRCN plans to update its submittal to summarize the results obtained during EQ testing.

Rolls-Royce Answer – Rolls-Royce intends to update the LTR and Commercial Grade Dedication Report after completion of the Supplemental Qualification Program, to reflect the results of the testing, as described in the Rolls-Royce letter dated September 15, 2011.

RAI-17: The RRCN "Qualification Test Specimen and Test System with System Specification for the Qualification Test Specimen and Data Acquisition System" (3 006 404 E) and the "Master Configuration List" (3 010 612 D) do not identify the software and hardware used for the Data Acquisition System (DAS). The "Qualification Test Specimen and Test System with System Specification for the Qualification Test Specimen and Data Acquisition System" (3 006 404 E) only describes requirements for the DAS. Further, during a presentation made to the NRC in January 2010, RRCN described that the DAS would be based on National Instruments PXI/SCXI data acquisition system. Please confirm the manufacturer and model number for the DAS equipment hardware and software.

Rolls-Royce Answer – The DAS is composed of the following equipment:
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Figure Q17-1 describes the hardware environment of the DAS.

Figure Q17-2 describes the software environment. The data exchanges between the software are as follows:
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The DAS-PC is developed with National Instruments LabWindows™/CVI Real-time application development tools.

The DAS-RT is developed with LabVIEW graphical programming environment and Real-time application development tools.

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Figure Q17-1: DAS Hardware Environment

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Figure Q17-2: DAS Software Environment

RAI-18: The EQ Plan (3 006 501 D), Pre-Qualification Acceptance Test Plan Section B.4 states that "the sequence of testing does not include Burn-In Testing as listed in Section 5.2.F of EPRI TR-107330." RRCN explained that the SPINLINE 3 platform manufacturing process includes routine burn-in of SPINLINE 3 platform hardware, and thus this will meet the intent of the EPRI TR-107330 requirement to detect early life failures during Pre-Qualification Testing through performance of burn-in testing. Please identify what documentation will be submitted to the NRC to evaluate compliance with burn-in test requirements, and describe the RRCN process used during "routine burn-in."

Rolls-Royce Answer – The purpose of the burn-in test is to detect any early life failures of the test specimen components. The acceptance criteria are defined that the test specimen shall pass the operability tests following the burn-in. It is noted that the response to any component failure during burn-in is to simply replace the component.

Section B.4 of the Equipment Qualification Plan states that the "the sequence of testing does not include Burn-In Testing as listed in Section 5.2.F of EPRI TR-107330." The RRCN ***SPINLINE 3*** platform manufacturing process includes routine burn-in of ***SPINLINE 3*** platform hardware. This process is documented in RRCN manufacturing procedures. Manufacturing burn-in of the ***SPINLINE 3*** QTS hardware is considered to meet the intent of the EPRI TR-107330 requirement to detect early life failures during Pre-Qualification Testing through performance of Burn-In Testing.

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Rolls-Royce only intends to provide the Equipment Qualification Test Summary Reports that will describe the results of Factory Acceptance Test, Pre-Qualification Acceptance Testing, and Qualification Testing described in the Equipment Qualification Plan.

Rolls-Royce notes that the position on burn-in testing taken in the ***SPINLINE 3*** Equipment Qualification Plan is consistent with the approach accepted by the NRC in the safety evaluation report issued for the TRICONEX Topical Report 7286-545-1-A in a NRC letter dated December 12, 2001.

RAI-19: The RRCN "Qualification Test Specimen and Test System with System Specification for the Qualification Test Specimen and Data Acquisition System" (3 006 404 E) Section 3.3.2.4 states that both ICTO pulse acquisition channels are used in the QTS, but only one channel is tested because the circuits are identical. Please clarify why both channels are used in the QTS. Also, describe what configuration represents the worst-case operating conditions for power/temperature loading.

Rolls-Royce Answer - The ICTO board is designed with two channels. Only one is tested because the circuits are identical; however, the two channels are used in the Qualification Test Specimen in order to test the worst operating conditions for power/temperature loading.

RAI-20: Section 4.3.4.4 of the LTR describes the operation modes for the pulse input (ICTO) acquisition board. Please explain if these modes will be tested during factory acceptance testing or equipment qualification testing.

Rolls-Royce Answer - The [[ ]] for the ICTO are tested during the factory acceptance testing and the equipment qualification testing.

The boundaries for the [[ ]] are shown in Figure 16 of the System Specification (3 006 404 E). The pulse input profiles used for the various test sequences are shown in Figure 22 of the same document.

The seismic and environmental test profiles toggle the pulse inputs between [[ ]] at the defined frequencies. These tests were performed as part of the factory acceptance testing and the equipment qualification testing.

The electromagnetic compatibility and channel accuracy test profiles toggle the pulse inputs [[ ]] at the defined frequencies. The [[ ]] These tests were performed as part of the equipment qualification testing.

RAI-21: The RRCN "Qualification Test Specimen and Test System with System Specification for the Qualification Test Specimen and Data Acquisition System" (3 006 404 E) Section 6.6 states that three parameters are stored in the CPU EEPROM. Please explain and describe these parameters and how they are used by the TSAP.

Rolls-Royce Answer – Three tuneable parameters are used in TSAP1 a parameters to control the time steps associated with certain analog output functions.

Tag Name	Default Value	Range	Type	Physical Unit	Function
TS1_PAR001	5	[1,10]	Integer	second	Analog output generation Out 2 time step
TS1_PAR002	5	[1,10]	Integer	second	Analog output generation Out 3 time step
TS1_PAR003	1	[1,10]	Integer	second	Analog output generation Out 5 time step

This information correlates with the time step information in Table 23 found in System Specification Section 6.7.2.1.

These parameters are sent by the TSAP over the network and checked against the expected values in DAS to validate proper functioning of the hardware associated with the tuneable parameters.

Verification of the correct time steps in DAS also demonstrates proper functioning of the hardware associated with the tuneable parameters.

RAI-22: Describe how the proposed approach for EQ will provide adequate assurance of operability for FPGA-programmed electronic boards in the SPINLINE 3 platform. Within this description clarify any role that application-specific System CGD is intended to contribute to assurance of operability.

Rolls-Royce Answer – The commercial grade dedication of the FPGA firmware is addressed in the response to RAI-5. The design process for the ***SPINLINE 3*** modules with FPGAs is described in the response to RAI-6. The commercial grade dedication approach to the ***SPINLINE 3*** platform (including modules with FPGAs) is described in the response to RAI-11. As noted in LTR Section 6.2.10, the logic in each of these components is standardized, and does not depend on any application-specific safety function being implemented in the ***SPINLINE 3*** system.

RAI-23: Describe all features of the test configuration that contribute to its behavior in response to detectable failures. This description should include, but not necessarily be limited to, its configured fail-safe states, the class of each detectable failure (fatal, vital, or non-vital), the ability of the self-testing to detect and report performance beyond specified operating tolerances, and the logic within its core logic board in response to detected failures.

Rolls-Royce Answer - Periodic testing of a ***SPINLINE 3*** safety platform is implemented to detect all failures that can render the equipment incapable of performing its function. Features that provide testability include self-diagnostic tests, surveillance functions, and periodic tests. The test strategy for ***SPINLINE 3*** is described in LTR Section 4.6.

The strategy for testing is based on considerations associated with the safety objectives of optimizing failure detection and avoidance of spurious trips and/or actuations. The testing strategy is based on a combination of the following:

- Self-diagnostic tests that run as part of each cycle,
- Surveillance functions that are performed by the MMU during plant operation, and
- Periodic tests that are performed during refueling outages.

When a fault is detected by self-diagnostic test, the output of the affected function is automatically set in a pre-determined safe position. For input boards, the result of a failure detected by a self-test is managed through the associated validity of the data and taken into account by the application software.

Self Test

The self test features of the ***SPINLINE 3*** equipment are described in LTR Sections 4.4.3.6, 4.5.4.2, 4.5.6, and 4.6.8. Generally, self-diagnostic tests are performed during each cyclic program execution. More details about self-test, valid and invalid data management, and operation modes are given in Sections 3, 4, and 5 of document ***SPINLINE 3*** / OSS / Software Requirement Specification (1 207 108 J), which was submitted to NRC by Rolls-Royce letter dated February 1, 2010.

Surveillance

The surveillance functions are based on analyzing data from the various ***SPINLINE 3*** equipment to indentify additional performance problems:
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Signaling

Alarm and signaling of failures detected by the self-test and surveillance functions are performed as described in LTR Sections 4.2.9 and 4.6.10.

Periodic Tests

The periodic tests are performed in steps, with overlapping between each step. The set of tests is a complete verification of all the hardware paths used by safety functions for actuation or signaling. The periodic tests have two main objectives:

- To demonstrate that the equipment is capable of operating correctly when needed. Therefore, periodic tests ensure that inputs and outputs are active and that each assembly can produce the right actuation control when required. The time between periodic tests is validated by the dependability assessment.
- To detect hardware latent faults in safety classified units, which are not detectable by self-diagnostic tests and by the self-supervision functions provided by the MMU. Generally, inputs and outputs of these Units are usually in the same state. During periodic tests, inputs are changed to cause expected changes in the output and thus to verify the capability of the system to operate.

The periodic tests are applied to each safety Unit by using an ATU. They are initiated manually, and then performed automatically.

The periodic tests are described in more detail in LTR Sections 4.6.7. The overlap of the self tests and periodic tests are shown in Figure Q23-1.

Validation of Self Test Behavior

The self tests are standard part of the ***SPINLINE 3*** technology and were developed and validated as described in LTR Section 6.2. These features were fully implemented in the QTS. Information on the validation testing performed on the ***SPINLINE 3*** self tests features are described in the following documents:

- ***SPINLINE 3*** / CSS / Software Integration Test Plan and Report (1 207 204 E) - Section 2.2.2.4 lists the test cases applied to the various input and output modules. The comment column identifies the test cases related to operating error identification. The results of the testing are summarized in Section 8.3.8.
- ***SPINLINE 3*** / OSS / Software Validation Test Plan (1 207 146 G) - Section 2.3 provides an overview of the testing preformed on the self-test features. Sections 4.5.2 (Self-tests in operation), 4.5.4 (Cycle time management), 4.5.5 (Short Pulse Tests), and 4.5.6 (I/O management) identify the test cases related to operating error identification.
- ***SPINLINE 3*** / OSS / Software Validation Test Report (1 207 232 F) - Sections 4.1.3 (I/O management), 4.2.2 (Self-tests in operation), 4.2.4 (Cycle time management), 4.3.4 (Short Pulse Tests), and 4.2.5 (I/O management) identify the test cases related to operating error identification. The results of the testing are summarized in Section 5.5.4.

These documents were submitted to NRC by Rolls-Royce letter dated February 1, 2010.

The periodic test functions for the QTS were performed by parts of the Operability Test Procedure (3 010 295 B), specifically the analog I/O accuracy test, response time test, discrete input operability test, and discrete output operability test.

The surveillance functions were not implemented for the qualification tests, since they were not applicable to the scope of the qualification testing.

Note: The statement in LTR Section 4.6.1 should be corrected as noted below:

The testing strategy is based on a combination of the following:

- Self-diagnostic tests that run as part of each cycle,
- Surveillance functions that are performed by the Monitoring and Maintenance Unit (MMU) during plant operation~~during refueling outages~~, and
- Periodic tests that are performed during refueling outages~~plant operation~~.

Note: The fourth column subheading in LTR Table 4.6-1 should be corrected to read: ~~Residual Failures Before~~ Periodic Test.

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Figure Q23-1: Periodic Test and Self Test Coverage

RAI-24: RRCN "Qualification Test Specimen and Test System with System Specification for the Qualification Test Specimen and Data Acquisition System" (3 006 404 E) Figure 14 shows the functional representation of I/O blocks in the QTS. Figure 17 shows a representation of the I/O for the TSAP. Please provide a brief description that relates these two figures, as well as their relationship with the functions in the TSAP.

Rolls-Royce Answer – The functional description of the QTS in the System Specification goes from the higher level description to the lower level requirements, which are necessary inputs to develop the software and the hardware. All the figures and tables explaining the functional description of the TSAP and DAS are introduced through Figure 13.

Figure 13 gives a global representation of physical connections between the QTS and the DAS. It also contains references to all the figures and tables that describe the TSAP and the DAS in the following sections in the System Specification. Figure 13 references Figure 14 for an expanded functional description of the QTS.

Figure 14 gives a functional representation of the QTS based on a representation of the hardware modules. Figure 14 includes a reference to Figure 17 for an expanded functional description of the TSAP. See the response to RAI-26 for a discussion of the TSAP.

The summary of I/O for TSAP and DAS are listed in System Specification Section 8.

RAI-25: Section 5.2.1.2 of the LTR describes the approach for evaluating the failure mode and effect analysis (FMEA) for a generic system. Table 5 of the Mapping of Generic SPINLINE 3 Licensing Documents to ISG-06 submitted on March 31, 2011, listed those documents that were submitted to the NRC on reliability analysis for each module in the SPINLINE 3 platform. Please clarify whether RRCN will perform a FMEA for the generic platform or whether the evaluation is only limited to the generic board-level FMEA.

Rolls-Royce Answer – As summarized in LTR Section 5.2.1, the hardware failure modes and effects were analyzed for each ***SPINLINE 3*** hardware module. The 12 generic board-level Reliability and Predictive Safety Analysis reports submitted to NRC by Rolls-Royce letter dated December 23, 2009 include board-level FMEAs. These board-level analyses are intended to be used as input data to support system level FMEA and reliability analyses for a plant-specific ***SPINLINE 3*** system, as noted in the Plant-Specific Action Item column for Items 2.8 and 2.15 in Table 1 of the Mapping of Generic ***SPINLINE 3*** Licensing Documents to ISG-06 submitted on March 31, 2011.

As noted in the response to RAI-2 above, the ***SPINLINE 3*** technology is modular in nature to meet various customer performance requirement while satisfying local regulatory requirements. There is no generic system architecture associated with the ***SPINLINE 3*** technology

As noted in the analyses for the ***SPINLINE 3*** boards, certain faults are only detectable at the system level and will rely on project-specific engineered monitoring and alarming features, as well as periodic surveillance testing.

Rolls-Royce does not intend to perform a generic system-level FMEA for the ***SPINLINE 3*** platform. Rolls-Royce also did not perform a system-level FMEA for the QTS, since the purpose of the QTS was only to support qualification of the ***SPINLINE 3*** modules. A FMEA for the QTS would not be representative of safety-system designed to meet IEEE Std 603 requirements and integrated with monitoring and alarm systems.

RAI-26: RRCN "Qualification Test Specimen and Test System with System Specification for the Qualification Test Specimen and Data Acquisition System" (3 006 404 E) Section 4.2.1.1 states that the TSAP is divided into two parts. Please provide the following information:

a. Explain how the TSAP is configured and divided
b. Describe the logic included in the TSAP for Processor Units (PU) 1 and 2 c. Provide a functional representation of the logic embedded in each PU

Rolls-Royce Answer to Part a) – The basic architecture of the TSAP is shown below in Figure Q26-1.

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Figure Q26-1: Basic TSAP Architecture

Rolls-Royce Answer to Part b) – The following functions are performed in TSAP1:
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Rolls-Royce Answer to Part c) – The high level functional representation of TSAP1 is shown in System Specification Figure 17 and the associated Quick Box descriptions. The main points of the functional representation are as follows:
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RAI-27: Equipment Qualification Plan (3 006 501 D) test plans provided in Appendices D3, E3, F3, etc., state that only one SPINLINE 3 QTS will be used during qualification. Please clarify your intent to use only one QTS. Nowhere within the Equipment Qualification Plan, the QTS, or the DAS System Specification is the use of one or more QTS mentioned.

Rolls-Royce Answer - Only one QTS was used in the ***SPINLINE 3*** qualification test program. The Appendices in the Equipment Qualification Plan specifically state:

> Due to the complexity of the hardware and the scope of the required qualification testing, only one ***SPINLINE 3*** QTS will be used during qualification testing.

This statement was made to address the issue raised in Regulatory Position C.2 of Regulatory Guide 1.209, which states:

> Although testing of a safety-related computer-based I&C system as a whole is preferred, type testing an entire system as a unit is not always practical. In those cases, confirmation of the dynamic response to the most limiting environmental and operational conditions for a computer-based I&C system is based on type testing of the individual modules and analysis of the cumulative effects of environmental and operational stress on the entire system.

The ***SPINLINE 3*** QTS conforms to the test specimen hardware configuration requirements defined in EPRI TR-107330 Section 6.2.1.

RAI-28: RRCN "Qualification Test Specimen and Test System with System Specification for the Qualification Test Specimen and Data Acquisition System" (3 006 404 E) Section 6.3 states that when an input signal is invalid, the TSAP will use the last valid value or state. Please explain how this will be processed and recorded by the DAS during EQ testing.

Rolls-Royce Answer - The ***SPINLINE 3*** system software supplies to the application a hardware validity indicator associated with each acquired data. It is invalid in the following cases:
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RAI-29: RRCN "Qualification Test Specimen and Test System with System Specification for the Qualification Test Specimen and Data Acquisition System" (3 006 404 E) Section 3.3.2.1 describes the temperature conditioning board. Section 3.3.4.2 states that the 8PT100 board is not connected to the backplane of PU2. Please describe how the temperature data simulated in the DAS would be transferred from the temperature conditioning board, processed by the 16EANA board, and sent to the CPU.

Rolls-Royce Answer - The RTD (8PT100) conditioning board is installed in a chassis dedicated to temperature conditioning. A power supply board connected to the backplane provides power supply distribution to the RTD board and its interface. There is no BAP bus on this backplane.

The RTD input signals are acquired by the I.8PT100 Interface board. The interface boards provide EMC filtering and RTD wiring connections (e.g., 3 or 4 wire). The signals are then routed to the 8PT100 conditioning board through a connector (XF2). The conditioning board performs signal conversion and conditioning. The resulting signal is then sent back to the interface board. The interface board output signal is then sent to an I.16EANA interface board as an analog input signal. The RTD signal input conditioning and subsequent analog signal processing is also described in the response to RAI-1.

RAI-30: RRCN "Qualification Test Specimen and Test System with System Specification for the Qualification Test Specimen and Data Acquisition System" (3 006 404 E) Section 3.3.6.1 describes the user interfaces included in the QTS. However, the test plans and procedures for EQ testing do not make reference to these interfaces. Please clarify if these interfaces would be used during EQ testing. If they are to be used, please explain how this will be accomplished.

Rolls-Royce Answer - Section 3.3.6.1 describes user interface features which are part ***SPINLINE 3*** platform design, which are implemented in the Qualification Test Specimen. The three main functions of the Operator Panel are:

- Periodic Testing: this function allows the operator to plug in an automatic tester which simulates/reads all inputs/outputs of the equipment
- Inhibition: this function allows the operator to force outputs to a specific status by powering off the corresponding output relays
- Reset: this function restores power to the corresponding output relays

Operator panel: this function consists in providing the operator with lamps, pushbuttons, switches for local monitoring and control for the inhibition function.

All of these features are implemented in the QTS, on the operator panel for local interface, and in the actuator driving assembly (refer to System Specification Section 3.3.2.5).

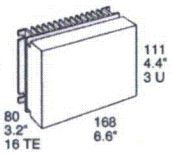
These features are not tested during qualification, as they are not safety functions. They have been implemented in the QTS specimen so as to prove that these functions, which are commonly implemented on ***SPINLINE 3*** systems, do not adversely affect the performances of the safety-related equipment during qualifications tests. Specifically, The MV16 includes a feature for inhibition of the control of the output relays. The inhibition is set by the maintenance operator from the operator panel during periodic test or maintenance. The test of the MV16 inhibition function will not be implemented in the qualification test. However, during the qualification tests, it will be verified that there is no spurious activation of the inhibition command.

One function is used during the performance of qualification tests:

- Reset Pushbutton (Operator panel): This function is required at each start-up sequence of the QTS, in order to activate the power-supply to the QTS relay outputs, to avoid any spurious command during the start-up sequence. After full QTS reset, the QTS relay outputs are still de-energized. The QTS start-up sequence requires the actuation of the Reset Pushbutton of the QTS operator panel to activate power supply to the QTS relay outputs. This feature is used to avoid any spurious command during the start-up sequence. On restoration of power, the QTS auxiliary power supply chassis outputs will return to nominal output voltage. (See Operability Test Procedure 3 010 295 B, Section 4).

Attachments

1. Rolls-Royce Procedure 8 303 314 L, Project Development Process
2. Rolls-Royce Procedure 8 303 334 F, System Design (Safety Systems)
3. Rolls-Royce Drawing 3008630 A (Sheet 6)
4. Power-One K Series with PFC Data Sheet, 150 – 280 Watt AC-DC Converters
5. Power-One P Series Data Sheet, 90 - 194 Watt DC-DC Converters
6. Microsens Ethernet Media Converter
7. Modicon Ethernet Cabling System Quick Reference Guide, Ethernet Hub 10 Mbps 3TP/2FL
8. Modicon Ethernet Cabling System Quick Reference Guide, Ethernet Hub 10 Mbps 4TP
9. Phoenix Contact FL MC 10/100 BASE-T/FO G1300ST Converter



RoHS Compliant

Features

Universal AC input range 100 - 240 VAC, 50 - 60 Hz
1 or 2 isolated outputs up to 56.5 VDC
Class I equipment

- RoHS lead-solder exemption compliant
- Power factor >0.93, harmonics IEC/EN 61000-3-2
- Output power up to 280 W
- Immunity according to IEC/EN 61000-4-2, -3, -4, -5, -6
- Emissions according to EN 55011/55022
- High efficiency
- Input over- and undervoltage lockout
- Adjustable output voltage with remote on/off
- Outputs: SELV, no load, overload, short-circuit proof
- Rectangular current limiting characteristic
- PCBs protected by lacquer
- Very high reliability

Safety according to IEC/EN 60950-1

Description

The LK 4000/5000 Series of AC-DC converters represents a flexible range of power supplies for use in advanced electronic systems; the LKP models are an extension with increased output power, but optimized to 230 VAC. Features include full power factor correction, good hold-up time, high efficiency and reliability, low output noise, and excellent dynamic response to load/line changes.

The converters are protected against surges and transients occurring at the source lines. Input over- and undervoltage lockout circuitry disables the outputs, when the input voltage is outside of the specified range. Input inrush current limitation is included for preventing circuit breakers and fuses from tripping at switch-on.

All outputs are overload, open- and short-circuit proof, and protected by a built-in suppressor diode. The outputs can be inhibited by a logic signal applied to connector pin 18. If the inhibit function is not used, pin 18 must be connected with pin 14 to enable the outputs.

LED indicators display the status of the converter and allow visual monitoring of the system at any time.

Full input to output, input to case, output to case and output to output isolation is provided. The converters are designed and built according to the international safety standards IEC/EN 60950-1. They have been approved by the safety agencies TÜV and UL (for USA and Canada).

The case design allows operation at nominal load up to 71 °C in a free air ambient temperature. If forced cooling is provided, the ambient temperature may exceed 71 °C, but the case temperature must remain below 95 °C under all conditions. However, higher output power up to 280 W is possible depending on environmental conditions and converter model.

An internal temperature sensor generates an inhibit signal, which disables the outputs, when the case temperature T_C exceeds the limit. The outputs automatically recover, when the temperature drops below the limit.

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Various options are available to adapt the converters to individual applications. An external temperature sensor is available to allow for temperature adapted battery charging.

The converters may either be plugged into 19" rack systems according to IEC 60297-3, or be mounted on a chassis or plate.

Important:

These products are intended to replace the LK1000 and LK2000 models, in order to comply with IEC/EN 61000-3-2. For applications with DC input or main frequencies other than 50/60 Hz, the LK1000 and LK2000 models are still available.

Model Selection

Non-standard input/output configurations or special customer adaptations are available on request.

Table 1: Standard models

Output 1 $V_{o\,nom}$ [VDC]	Output 1 $I_{o\,nom}$ [A]	Output 2 $V_{o\,nom}$ [VDC]	Output 2 $I_{o\,nom}$ [A]	Operating input range $V_{i\,min}$ – $V_{i\,max}$ [VAC]	Type designation	Efficiency[1] η_{min} [%]	Options
5.1	25	–	–	85 – 264	LK4003-6R	78	E, P, D, V[2], P, T, K[5], B1, B2[4]
12	12	–	–	85 – 264	LK4301-7R	84	-9E, P, D, T, B1, B2[4]
15	10	–	–		LK4501-7R	85	
24	6	–	–		LK4601-7R	86	
12	6	12[3]	6	85 – 264	LK5320-7R	82	-9E, P, D, T, B1, B2[4]
15	5	15[3]	5		LK5540-7R	83	
24	3	24[3]	3		LK5660-7R	83	
24	5.2	24[3]	5.2	187 – 255	LKP5660-7R	86	-9E, P, D, T, B1, B2[4]
24	5.8	24[3]	5.8		LKP5661-5R	86	E, P, D, T, B1, B2[4]

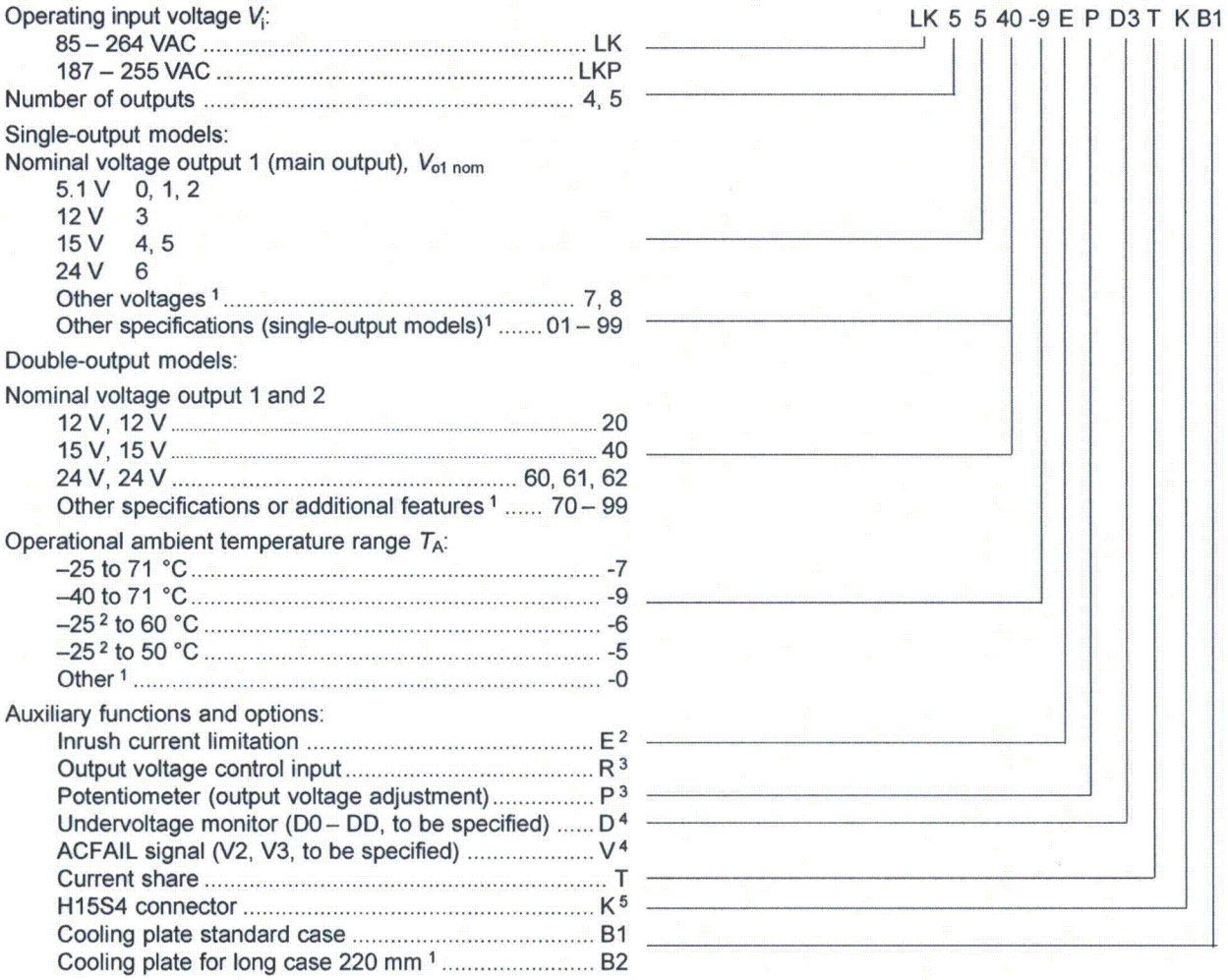
[1] Min. efficiency at $V_{i\,nom}$, $I_{o\,nom}$ and T_A = 25 °C. Typical values are approximately 2% better.
[2] Option V for models with 5.1 V outputs; excludes option D
[3] Second output semi-regulated
[4] For customer-specific models with 220 mm case length
[5] For new designs, use only option K.

Table 2: Battery charger models

Nom. output values $V_{o\,nom}$ [VDC]	Nom. output values $I_{o\,nom}$ [A]	Output range[5] $V_{o\,min}$ – $V_{o\,max}$ [VDC]	Operating input range $V_{i\,min}$ – $V_{i\,max}$ [VAC]	Type designation	Efficiency[1] η_{min} [%]	Options
12.84	10	12.62 – 14.12	85 – 264	LK4740-7R	84	-9E, D, T, B1, B2[4]
25.68[2]	5.4	25.25 – 28.25		LK5740-7R	83	
51.36[3]	2.7	25.5 – 56.5		LK5740-7R	83	
25.68[2]	9	25.25 – 28.25	187 – 255	LKP5740-7R	86	-9E, D, T, B1, B2[4]
25.68[2]	10	25.25 – 28.25		LKP5741-5R	86	E, D, T, B1, B2[4]
51.36[3]	4.5	50.5 – 56.5	187 – 255	LKP5740-7R	86	-9E, D, T, B1, B2[4]
51.36[3]	5	50.5 – 56.5		LKP5741-5R	85	E, D, T, B1, B2[4]

[1] Min. efficiency at $V_{i\,nom}$, $I_{o\,nom}$ and T_A = 25 °C. Typical values are approximately 2% better.
[2] Both outputs connected in parallel
[3] Both outputs connected in series
[4] For customer-specific models with 220 mm case length
[5] Controlled by the battery temperature sensor, see *Accessories*

Part Number Description



Operating input voltage V_i:
- 85 – 264 VAC ..... LK
- 187 – 255 VAC ..... LKP

Number of outputs 4, 5

Single-output models:

Nominal voltage output 1 (main output), $V_{o1\ nom}$
- 5.1 V 0, 1, 2
- 12 V 3
- 15 V 4, 5
- 24 V 6
- Other voltages [1] 7, 8
- Other specifications (single-output models)[1] ..... 01 – 99

Double-output models:

Nominal voltage output 1 and 2
- 12 V, 12 V 20
- 15 V, 15 V 40
- 24 V, 24 V 60, 61, 62
- Other specifications or additional features [1] ..... 70 – 99

Operational ambient temperature range T_A:
- –25 to 71 °C ..... -7
- –40 to 71 °C ..... -9
- –25 [2] to 60 °C ..... -6
- –25 [2] to 50 °C ..... -5
- Other [1] ..... -0

Auxiliary functions and options:
- Inrush current limitation ..... E [2]
- Output voltage control input ..... R [3]
- Potentiometer (output voltage adjustment) ..... P [3]
- Undervoltage monitor (D0 – DD, to be specified) ..... D [4]
- ACFAIL signal (V2, V3, to be specified) ..... V [4]
- Current share ..... T
- H15S4 connector ..... K [5]
- Cooling plate standard case B1
- Cooling plate for long case 220 mm [1] B2

[1] Customer-specific models
[2] Option E is mandatory for all -9 models. Models with -5E or -6E are functional down to –40 °C.
[3] Feature R excludes option P and vice versa. Option P is not available for battery charger models.
[4] Option D excludes option V and vice versa; option V is available for models with 5.1 V output only (LK4003, etc.).
[5] Option K is available for models with 5.1 V output only (LK4003, etc.) to ensure compatibility with LK1001 models.

Example: LK5540-9EPD3TB1: Power factor corrected AC-DC converter, operating input voltage range 85 – 264 VAC, 2 electrically isolated outputs, each providing 15 V, 5 A, equipped with inrush current limiter, a potentiometer to adjust the output voltages, undervoltage monitor D3, current share feature, and a cooling plate B1.

Product Marking

Basic type designation, applicable approval marks, CE mark, warnings, pin designation, Power-One patents and company logo, identification of LEDs, test sockets, and potentiometer.

Specific type designation, input voltage range, nominal output voltages and currents, degree of protection, batch no., serial no., and data code including production site, modification status, and date of production.

Functional Description

The input voltage is fed via an input fuse, an input filter, a rectifier, and an inrush current limiter to a boost converter. This step-up converter provides a sinusoidal input current (IEC/EN 61000-3-2, class D equipment) and charges the bulk capacitor C_i to approx. 370 VDC. This capacitor sources a single-transistor forward converter and provides the power during the hold-up time.

Each output is powered by a separate secondary winding of the main transformer. The resultant voltages are rectified and their ripple smoothed by a power choke and an output filter. The control logic senses the main output voltage V_{o1} and generates, with respect to the maximum admissible output currents, the control signal for the switching transistor of the forward converter.

The second output of double output models is tracking to the main output, but has its own current limiting circuit. If the main output voltage drops due to current limitation, the second output voltage will fall as well and vice versa.

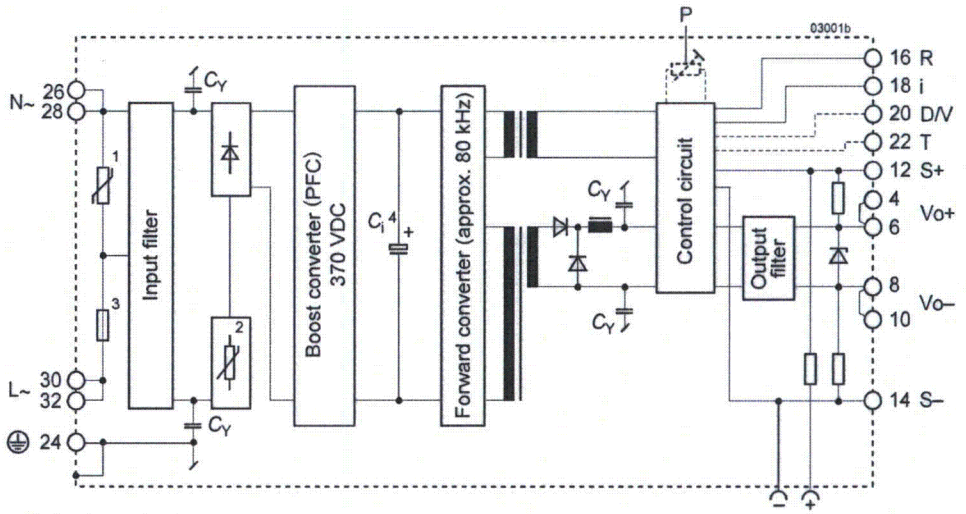


Fig. 1
Block diagram of single-output converters

1 Transient suppressor (VDR)
2 Inrush current limiter (NTC, only models with $T_{A\,min}$ = –25 °C), or option E
3 Input fuse
4 Bulk capacitor (C_i)

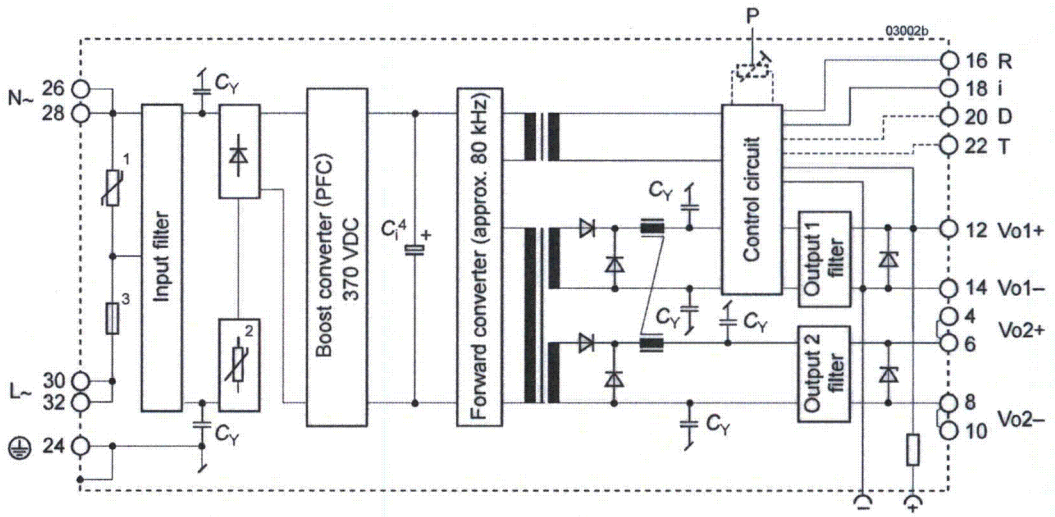


Fig. 2
Block diagram of double-output models

1 Transient suppressor (VDR)
2 Inrush current limiter (NTC, only models with $T_{A\,min}$ = –25 °C), or option E
3 Input fuse
4 Bulk capacitor (C_i)

Electrical Input Data

General Conditions:

- T_A = 25 °C, unless T_C is specified.
- Pin 18 connected to pin 14, R input not connected, V_o adjusted to $V_{o\,nom}$ (option P)
- Sense line pins S+ and S– connected to Vo+ and Vo–, respectively.

Table 3: Electrical input data

Input			LK			LKP			
Characteristics		**Conditions**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**
V_i	Rated input voltage range	I_o = 0 – $I_{o\,nom}$ $T_{C\,min}$ to $T_{C\,max}$	100		240	200		240	VAC[1]
$V_{i\,op}$	Operating input voltage range		85		264	187		255	
$V_{i\,nom}$	Nominal input voltage	50 – 60 Hz		230			230		
I_i	Input current	$V_{i\,nom}$, $I_{o\,nom}$ [2]		0.8			1.25		A
P_{i0}	No-load input power	$V_{i\,min}$ – $V_{i\,max}$, I_o = 0		9	10		9	10	W
$P_{i\,inh}$	Idle input power	converter inhibited		3.5	5		3.5	5	
R_i	Input resistance		480			480			mΩ
R_{NTC}	NTC resistance (see fig. 3)[3]	conv. not operating	3200	4000		3200	4000		
C_i	Input capacitance		80	100	120	110	136	165	µF
$V_{i\,RFI}$	Conducted input RFI	EN 55011/55022 $V_{i\,nom}$, $I_{o\,nom}$		B			B		
	Radiated input RFI			A			B		
$V_{i\,abs}$	Input voltage limits without damage				283			283	VAC
			–400		400	–400		400	VDC[4]

[1] Rated input frequency: 50 – 60 Hz, operating frequency range: 47 – 63 Hz. For operation at other frequencies, contact Power-One.
[2] With double-output models, both outputs loaded with $I_{o\,nom}$
[3] Valid for models without option E. This is the NTC resistance value at 25 °C and applies to cold converters for the initial switch-on cycle. Subsequent switch-on/off cycles increase the inrush current peak value.
[4] Operation with DC input voltage is not specified and not recommended.

Input Transient Protection

A VDR together with the input fuse and a symmetrical input filter form an effective protection against high input transient voltages.

Input Fuse

A fuse mounted inside the converter in series to the phase line protects against severe defects. A second fuse in the neutral line may be necessary in certain applications; see *Installation Instructions*.

Table 4: Fuse specification

Model	Fuse type	Fuse rating
LK4/5000	slow-blow	SP T, 4 A, 250 V, 5 × 20 mm
LKP	slow-blow	SP T, 4 A, 250 V, 5 × 20 mm

Input Under-/Overvoltage Lockout

If the input voltage remains below approx. 65 VAC (LKP: 150 VAC) or exceeds $V_{i\,abs}$, an internally generated inhibit signal disables the output(s). Do not check the overvoltage lockout function!

If V_i is below $V_{i\,min}$, but above the undervoltage lockout level, the output voltage may be below the value specified in the tables *Electrical Output Data*.

Inrush Current Limitation

The models without option E incorporate an NTC resistor in the input circuitry, which at initial turn-on reduces the peak inrush current value by a factor of 5 to 10 to protect connectors and switching devices from damage. Subsequent switch-on cycles within short periods will cause an increase of the peak inrush current value due to the warming-up of the NTC resistor.

The inrush current peak value (initial switch-on cycle) can be determined by following calculation:

$$I_{inr\,p} = \frac{V_i \cdot \sqrt{2}}{(R_{s\,ext} + R_i + R_{NTC})}$$

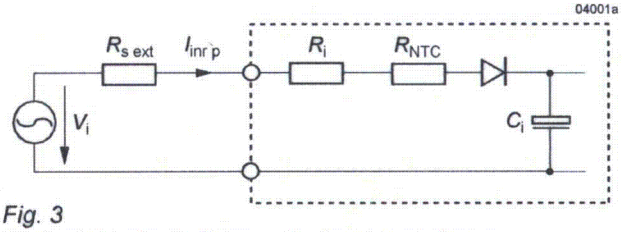


Fig. 3
Equivalent circuit diagram for input impedance.

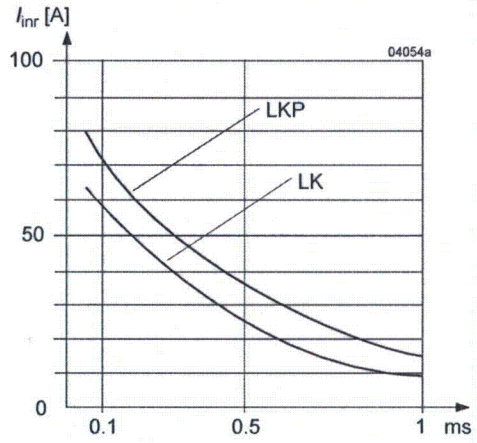


Fig. 4
Theoretical worst case input inrush current versus time at V_i = 255 V, R_{ext} = 0 for models without feature E

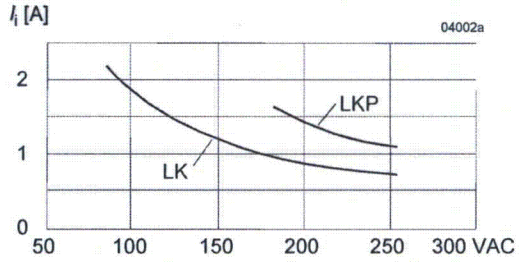


Fig. 5
Input current versus input voltage at $I_{o\ nom}$

Power Factor and Harmonics

Power factor correction is achieved by controlling the input current waveform synchronously with the input voltage waveform. The power factor control is active under all operating conditions.

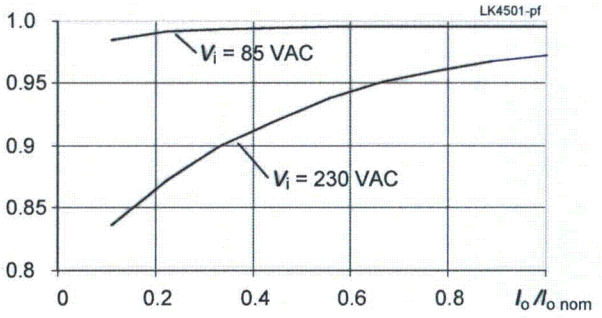


Fig. 6
Power factor versus output current (LK4501-7R)

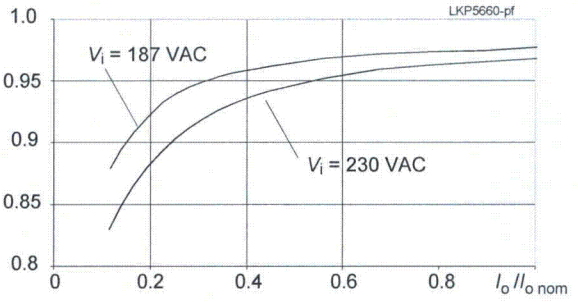


Fig. 7
Power factor versus output current (LKP5660-7R)

The harmonic distortion is well below the limits specified in IEC/EN 61000-3-2, class D, see fig. below:

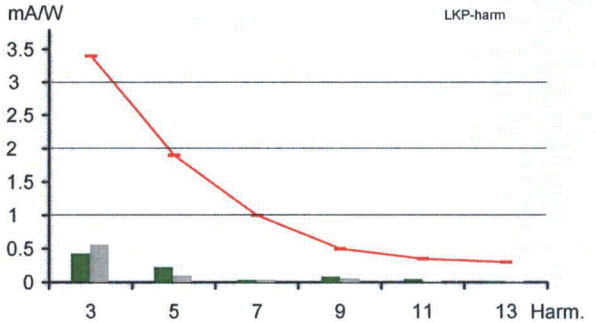


Fig. 8
Harmonic input currents at V_i = 230 V, $I_o = I_{o\ nom}$ for LK4501-7R (left bars) and LKP5660-7R.

Switching Frequency

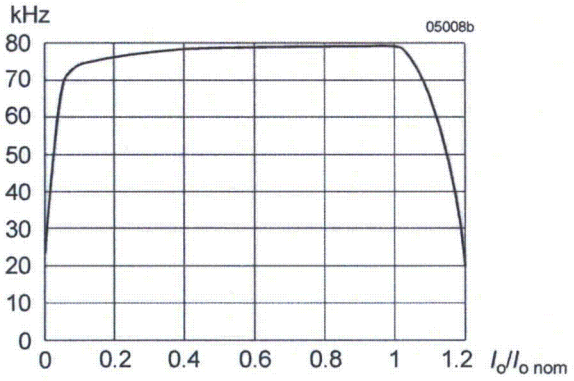


Fig. 9
Typical inverter switching frequency versus load. The boost converter at the input stage operates with a constant switching frequency of 100 kHz.

Hold-up Time

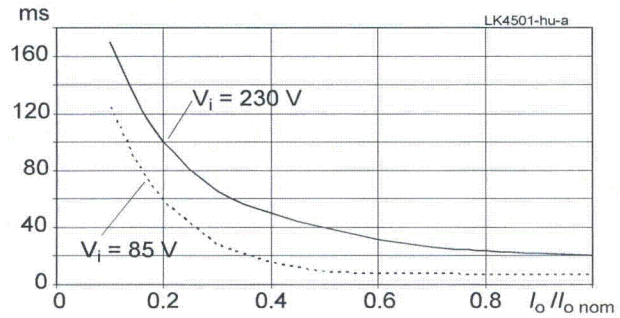


Fig. 10a
Hold-up time versus output power (LK4501-7R), valid for converters with version V102 or higher.

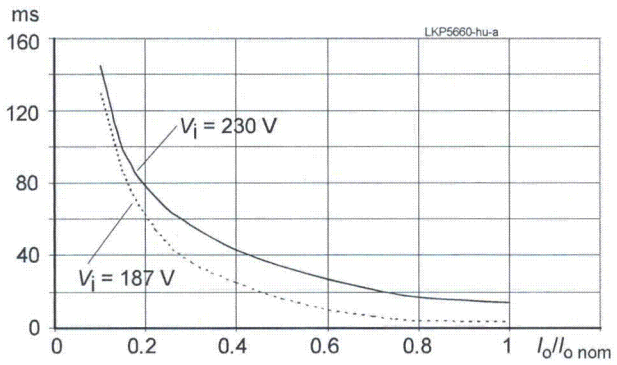


Fig. 10b
Hold-up time versus output power (LKP5660-7R)

Efficiency

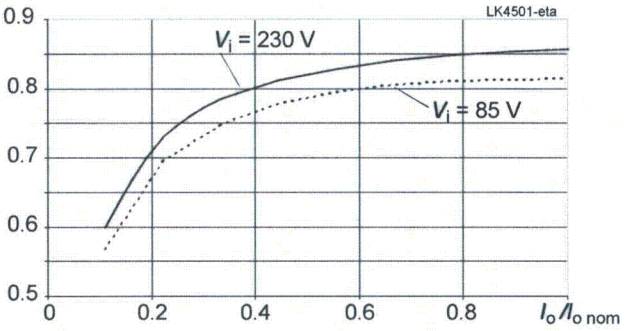


Fig. 11a
Efficiency versus output current (LK4501-7R)

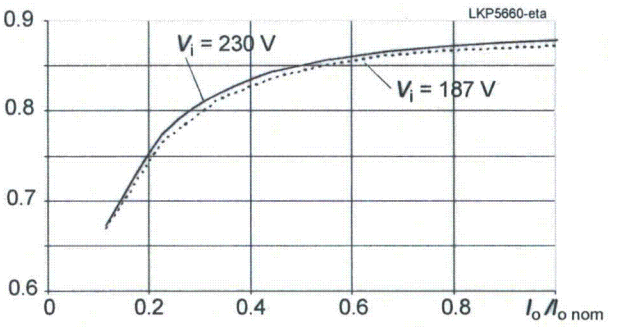


Fig. 11b
Efficiency versus output current (LKP5660-7R)

Electrical Output Data

General Conditions:
– T_A = 25 °C, unless T_C is specified.
– Pin 18 (i) connected to pin 14 (S– or Vo1–), R input not connected, V_o adjusted to $V_{o\,nom}$ (option P),
– Sense line pins 12 (S+) and 14 (S–) connected to pins 4 (Vo1+) and 8 (Vo1–), respectively.

Table 5: Output data of single-output models

Output				LK4003-6 5.1 V			LK4301 / 4740[5] 12 V[5]			LK4501 15 V			LK4601 24 V			
Characteristics			**Conditions**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Unit**
V_o	Output voltage		$V_{i\,nom}$, $I_{o\,nom}$	5.05		5.15	11.88[5]		12.12[5]	14.85		15.15	23.76		24.24	V
$V_{o\,BR}$	Overvoltage protection (suppressor diode)[6]			6			15.2/17[5]			19.6			28.5			
$I_{o\,nom}$	Output current nom.[1]		$V_{i\,min}$ – $V_{i\,max}$ $T_{C\,min}$ – $T_{C\,max}$		25			12/10[5]			10			6		A
I_{oL}	Output current limit[2]		$V_{i\,min}$ – $V_{i\,max}$	26			12.2			10.2			6.2			
v_o	Output noise[3]	Low frequency	$V_{i\,nom}$, $I_{o\,nom}$		2			2			2			2		mV_{pp}
		Switching frequ.	BW = 20 MHz		15			5			5			5		
		Total incl. spikes			25			40			40			40		
$\Delta V_{o\,u}$	Static line regulation with respect to $V_{i\,nom}$		$V_{i\,min}$ – $V_{i\,max}$ $I_{o\,nom}$			±5			±12			±15			±24	mV
$\Delta V_{o\,l}$	Static load regulation		$V_{i\,nom}$ (0.1 – 1) $I_{o\,nom}$			–15			–25			–30			–40	
$v_{o\,d}$	Dynamic load regulat.[2]	Voltage deviation[2]	$V_{i\,nom}$ $I_{o\,nom} \leftrightarrow$ ½ $I_{o\,nom}$		±100			±100			±100			±100		
t_d		Recovery time[2]			0.3			0.4			0.4			0.3		ms
$\alpha_{v\,o}$	Temperature coefficient of output voltage[4]		$T_{C\,min}$ – T_{Cmax} $I_{o\,nom}$		±0.02			±0.02			±0.02			±0.02		%/K

[1] If the output voltages are increased above $V_{o\,nom}$ through R-input control, option P setting, remote sensing or option T, the output currents should be reduced accordingly so that $P_{o\,nom}$ is not exceeded.
[2] See *Output Voltage Regulation*
[3] Measured according to IEC/EN 61204 with a probe according to annex A
[4] For battery charger applications, a defined negative temperature coefficient can be provided by using a temperature sensor (see *Accessories*), but we recommend choosing special battery charger models.
[5] Especially designed for battery charging using the temperature sensor (see *Accessories*). V_o is set to 12.84 V ±1% (R-input open)
[6] Breakdown voltage of the incorporated suppressor diode (1 mA; 10 mA for 5 V output). To exceed $V_{o\,BR}$ is dangerous for the suppressor diode.

Table 6a: Output data of double-output LK models. General conditions as in table 5.

Output				LK5320 2 × 12 V						LK5540 2 × 15 V						
Characteristics			Conditions	Output 1			Output 2			Output 1			Output 2			Unit
				min	typ	max	min	typ	max	min	typ	max	min	typ	max	
V_o	Output voltage		$V_{i\,nom}$, $I_{o\,nom}$ [1]	11.88		12.12	11.76		12.24	14.85		15.15	14.70		15.30	V
$V_{o\,BR}$ [8]	Overvoltage protection (suppressor diode)			15.2			15.2			19.6			19.6			
$I_{o\,nom}$	Output current nom. [2]		$V_{i\,min} - V_{i\,max}$ $T_{C\,min} - T_{C\,max}$		6			6			5			5		A
I_{oL}	Output current limit [5]		$V_{i\,min} - V_{i\,max}$	6.2			6.2			5.2			5.2			
v_o	Output noise [3]	Low frequency	$V_{i\,nom}$, $I_{o\,nom}$ BW = 20 MHz		3			3			3			3		mV_{pp}
		Switching freq.			12			12			10			10		
		Total incl. spikes			70			60			80			60		
$\Delta V_{o\,u}$	Static line regulation with respect to $V_{i\,nom}$		$V_{i\,min} - V_{i\,max}$ $I_{o\,nom}$			±12		[5]				±15		[5]		mV
$\Delta V_{o\,l}$	Static load regulation [1]		$V_{i\,nom}$ (0.1 – 1) $I_{o\,nom}$			–40		[5]				–50		[5]		
$v_{o\,d}$	Dynamic load regulat. [3]	Voltage deviation [4]	$V_{i\,nom}$, $I_{o1\,nom} \leftrightarrow ½\ I_{o1\,nom}$		±100			±150			±100			±150		
t_d		Recovery time [4]	½ $I_{o2\,nom}$		0.3						0.4					ms
$\alpha_{v\,o}$	Temperature coefficient of output voltage [6]		$T_{C\,min} - T_{C\,max}$ $I_{o\,nom}$		±0.02						±0.02					%/K

Table 6b: Output data of double-output LK models. General conditions as in table 5.

Output				LK5660 / 5740 [7] 2 × 24 V / 25.68 V [7]						
Characteristics			Conditions	Output 1			Output 2			Unit
				min	typ	max	min	typ	max	
V_o	Output voltage		$V_{i\,nom}$, $I_{o\,nom}$ [1]	23.76 [7]		24.24 [7]	23.52 [7]		24.48 [7]	V
$V_{o\,BR}$ [8]	Overvoltage protection (suppressor diode)			28.5/34 [7]			28.5/34 [7]			
$I_{o\,nom}$	Output current nom. [2]		$V_{i\,min} - V_{i\,max}$ $T_{C\,min} - T_{C\,max}$		3 / 2.7 [7]			3 / 2.7 [7]		A
I_{oL}	Output current limit [5]		$V_{i\,min} - V_{i\,max}$	3.2			3.2			
v_o	Output noise [3]	Low frequency	$V_{i\,nom}$, $I_{o\,nom}$ BW = 20 MHz		3			3		mV_{pp}
		Switching freq.			10			10		
		Total incl. spikes			80			60		
$\Delta V_{o\,u}$	Static line regulation with respect to $V_{i\,nom}$ [3]		$V_{i\,min} - V_{i\,max}$ $I_{o\,nom}$			±20		[5]		mV
$\Delta V_{o\,l}$	Static load regulation [1]		$V_{i\,nom}$ (0.1 – 1) $I_{o\,nom}$			–40		[5]		
$v_{o\,d}$	Dynamic load regulat. [3]	Voltage deviation [4]	$V_{i\,nom}$ $I_{o1\,nom} \leftrightarrow ½\ I_{o1\,nom}$		±100			±150		
t_d		Recovery time [4]	½ $I_{o2\,nom}$		0.3					ms
$\alpha_{v\,o}$	Temperature coefficient of output voltage [6]		$T_{C\,min} - T_{C\,max}$ $I_{o\,nom}$		±0.02					%/K

1 Same conditions for both outputs
2 If the output voltages are increased above $V_{o\,nom}$ via R-input control, option P setting, remote sensing or option T, the output currents should be reduced accordingly so that $P_{o\,nom}$ is not exceeded.
3 Measured according to IEC/EN 61204 with a probe annex A
4 See *Dynamic Load Regulation*
5 See *Output Voltage Regulation of Double-Output Models*
6 For battery charger applications a defined negative temperature coefficient can be provided by using a temperature sensor; see *Accessories*.
7 Especially designed for battery charging using the battery temperature sensor; see *Accessories*.
V_{o1} is set to 25.68 V ±1% (R-input open).
8 Breakdown voltage of the incorporated suppressor diodes (1 mA). To exceed $V_{o\,BR}$ is dangerous for the suppressor diodes.

Table 7a: Output data of double-output LKP models. General conditions as in table 5.

Output				LKP5660-7 2× 24 V						LKP5740-7 [7] 2× 25.68 V						Unit
Characteristics Conditions				Output 1			Output 2			Output 1			Output 2			
				min	typ	max	min	typ	max	min	typ	max	min	typ	max	
V_o	Output voltage		$V_{i\,nom}$, $I_{o\,nom}$ [1]	23.76		24.24	23.52		24.48	25.42		25.93	25.17		26.19	V
$V_{o\,BR}$ [8]	Overvoltage protection (suppressor diode)			28.5			28.5			34			34			
$I_{o\,nom}$	Output current nom. [2] $T_{C\,min} - T_{C\,max}$		$V_{i\,min} - V_{i\,max}$	5.2			5.2			4.5			4.5			A
I_{oL}	Output current limit [5]		$V_{i\,min} - V_{i\,max}$	5.3			5.3			4.6			4.6			
v_o	Output noise [3]	Low frequency	$V_{i\,nom}$, $I_{o\,nom}$ BW = 20 MHz		10			10			10			10		mV_{pp}
		Switching freq.			20			20			20			20		
		Total incl.spikes			120			40			120			100		
$\Delta V_{o\,u}$	Static line regulation with respect to $V_{i\,nom}$		$V_{i\,min} - V_{i\,max}$ $I_{o\,nom}$			±10		[5]				±10		[5]		mV
$\Delta V_{o\,l}$	Static load regulation (0.1 – 1) $I_{o\,nom}$		$V_{i\,nom}$			−60		[5]				−80		[5]		
$v_{o\,d}$	Dynamic load regulat. [3]	Voltage deviation [4]	$V_{i\,nom}$ $I_{o\,nom} \leftrightarrow {}^1/_2\, I_{o\,nom}$		±150			±150			±150			±150		
t_d		Recovery time [4]			0.3						0.4					ms
$\alpha_{v\,o}$	Temperature coefficient of output voltage [6]		$T_{C\,min} - T_{C\,max}$ $I_{o\,nom}$		±0.02						±0.02					%/K

[1] Same conditions for both outputs
[2] If the output voltages are increased above $V_{o\,nom}$ via R-input control, option P setting, remote sensing or option T, the output currents should be reduced accordingly so that $P_{o\,nom}$ is not exceeded.
[3] Measured according to IEC/EN 61204 with a probe according to annex A
[4] See *Dynamic Load Regulation*
[5] See *Output Voltage Regulation of Double-Output Models*
[6] For battery charger applications, a defined negative temperature coefficient can be provided by using a temperature sensor (see *Accessories*), but we recommend choosing special battery charger models.
[7] Especially designed for battery charging using the battery temperature sensor (see *Accessories*). Similar models see table 7b. V_{o1} is set to 25.68 V ±1% (R-input open).
[6] Breakdown voltage of the incorporated suppressor diodes (1 mA). To exceed $V_{o\,BR}$ is dangerous for the suppressor diodes.

Table 7b: Other LKP models

All data not specified in this table are equal to LKP5740-7. General conditions as in table 5.

Output			LKP5661-5[7] 2× 24 V						LKP5741-5[8] 2× 25.68 V						Unit
Characteristics		Conditions	Output 1			Output 2			Output 1			Output 2			
			min	typ	max	min	typ	max	min	typ	max	min	typ	max	
$I_{o\,nom}$	Output current nom	$V_{i\,min} - V_{i\,max}$ $T_{C\,min} - T_{C\,max}$		5.8			5.8			5			5		A
I_{oL}	Output current limit [1]	$V_{i\,min} - V_{i\,max}$	6.0			6.0			5.2			5.2			
$T_{A\,max}$	Max. operating temp.			50						50					°C

[7] All other data see LKP5660-7
[8] All other data see LKP5740-7 (battery charger)

Thermal Considerations

If a converter is located in free, quasi-stationary air (convection cooling) at the indicated maximum ambient temperature $T_{A\,max}$ (see table: *Temperature specifications)* and is operated at its nominal input voltage and output power, the temperature measured at the *Measuring point of case temperature* T_C (see: *Mechanical Data*) will approach the indicated value $T_{C\,max}$ after the warm-up phase. However, the relationship between T_A and T_C depends heavily on the conditions of operation and integration into a system. The thermal conditions are influenced by input voltage, output current, airflow, and temperature of surrounding components and surfaces. $T_{A\,max}$ is therefore, contrary to $T_{C\,max}$, an indicative value only.

Caution: The installer must ensure that under all operating conditions T_C remains within the limits stated in the table: *Temperature specifications.*

Notes: Sufficient forced cooling or an additional heat sink (applied to -7 or -9) models allows T_A to be higher than 71 °C (e.g., 85 °C), if $T_{C\,max}$ is not exceeded. Details are specified in fig. 12, including -5 and -6 models.

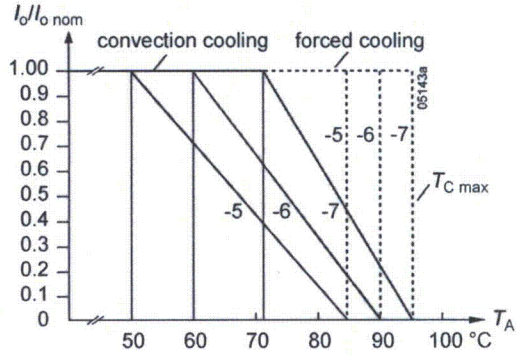


Fig. 12
Output current derating versus temperature for -5, -6, and -7 (equal to -9) models.

Thermal Protection

A temperature sensor generates an internal inhibit signal, which disables the outputs, when the case temperature exceeds $T_{C\,max}$. The outputs automatically recover, when the temperature drops below this limit.

Continuous operation under simultaneous extreme worst-case conditions of the following three parameters should be avoided: Minimum input voltage, maximum output power, and maximum temperature.

Output Protection

Each output (and the connected equipment) is protected by a suppressor diode against overvoltage, which could occur due to a failure of the control circuit. In such a case, the suppressor diode becomes a short circuit. The suppressor diodes may smooth short overvoltages resulting from dynamic load changes, but they are not designed to withstand externally applied overvoltages.

A short circuit at any of the two outputs will cause a shut-down of the other output. A red LED indicates an overload condition.

Note: $V_{o\,BR}$ is specified in *Electrical Output Data*. If this voltage is exceeded, the suppressor diode generates losses and may become a short circuit.

Parallel or Series Connection of Converters

Single or double-output models with equal output voltage can be connected in parallel without any precautions using option T (current sharing). If the T pins are interconnected, all converters share the output current equally.

Single-output models and/or main and second outputs of double-output models can be connected in series with any other (similar) output.

Notes:

- Parallel connection of double-output models should always include both, main and second output to maintain good regulation of both outputs.
- Not more than 5 converters should be connected in parallel.
- Series connection of second outputs without involving their main outputs should be avoided as regulation may be poor.
- Models with a rated output voltage above 36 V need additional measures to comply with the requirements of SELV (Safe Extra Low Voltage).
- The maximum output current is limited by the output with the lowest current limitation, if several outputs are connected in series.

Output Voltage Regulation

The following figures apply to single-output or double-output models with parallel-connected outputs.

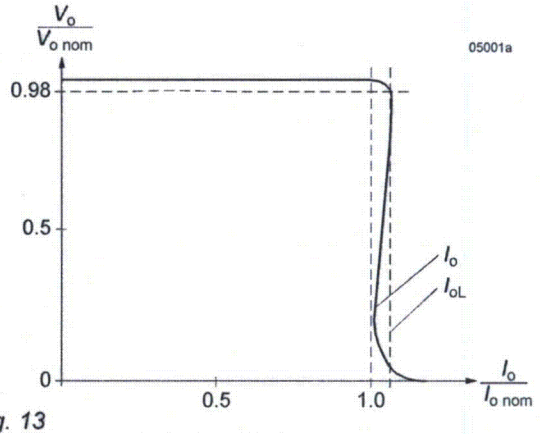


Fig. 13
Typical output characteristic V_o versus I_o.

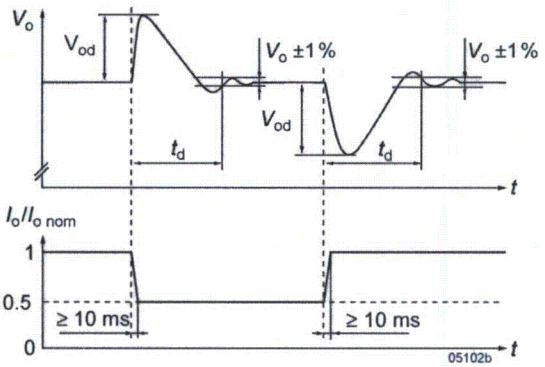


Fig. 14
Typical dynamic load regulation of V_o.

Output Regulation of Double-Output Models

Output 1 is under normal conditions regulated to $V_{o\,nom}$, independent of the output currents.

V_{o2} depends upon the load distribution. If both outputs are loaded with more than 10% of $I_{o\,nom}$, the deviation of V_{o2} remains within ±5% of V_{o1}. The following 3 figures show the regulation with varying load distribution.

Two outputs of a double-output model connected in parallel behave like the output of a single-output model.

Note: If output 2 is not used, we recommend connecting it in parallel with output 1. This ensures good regulation and efficiency.

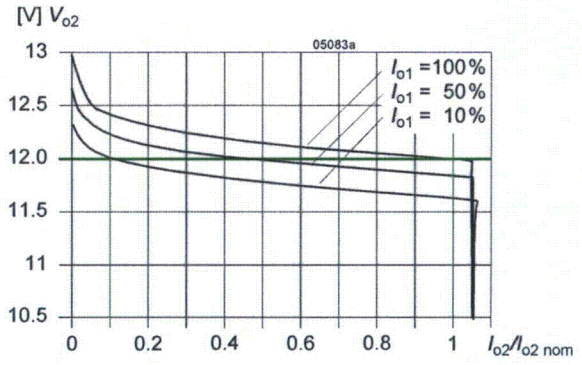


Fig. 15
Models with 2 outputs 12 V: ΔV_{o2} versus I_{o2} with various I_{o1} (typ).

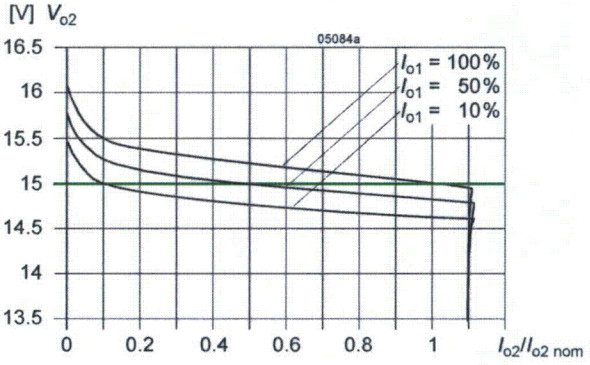


Fig. 16
Models with 2 outputs 15 V: ΔV_{o2} versus I_{o2} with various I_{o1} (typ).

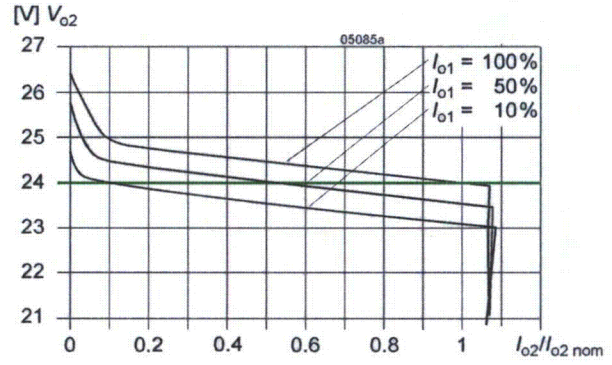


Fig. 17
Models with 2 outputs 24 V: ΔV_{o2} versus I_{o2} with various I_{o1} (typ).

Auxiliary Functions

Inhibit for Remote On/Off

The outputs may be enabled or disabled by means of a logic signal (TTL, CMOS, etc.) applied between the inhibit input i and pin 18 (S– or Vo1–). In systems with several converters, this feature can be used to control the activation sequence of the converters. If the inhibit function is not required, connect the inhibit pin 18 to pin 14.

Note: If pin 18 is not connected, the output is disabled.

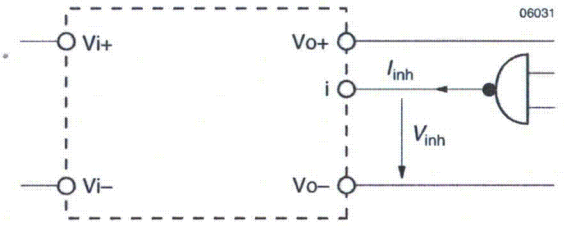


Fig. 18
Definition of V_{inh} and I_{inh}.

Table 8: Inhibit characteristics

Characteristic			Conditions	min	typ	max	Unit
V_{inh}	Inhibit voltage	V_o = on	$V_{i\,min} - V_{i\,max}$	–50		0.8	V
		V_o = off		2.4		50	
I_{inh}	Inhibit current		V_{inh} = 0			–400	µA
t_r	Rise time				30		ms
t_f	Fall time		depending on I_o				

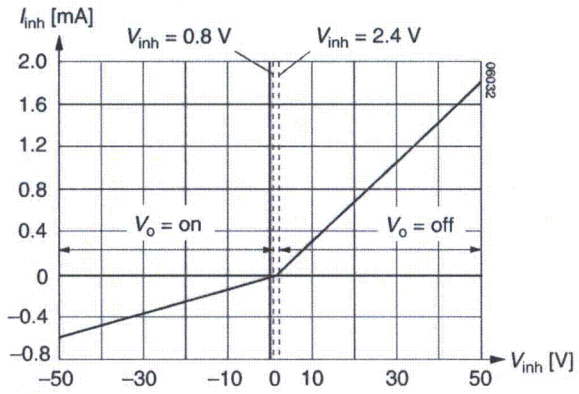


Fig. 19
Typical inhibit current I_{inh} versus inhibit voltage V_{inh}

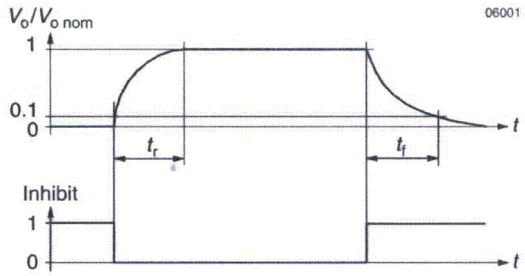


Fig. 20
Output response as a function of inhibit control

Sense Lines (Single-Output Models)

Important: Sense lines must always be connected! Incorrectly connected sense lines may activate the overvoltage protection resulting in a permanent short-circuit of the output.

This feature allows for compensation of voltage drops across the connector contacts and if necessary, across the load lines. We recommend connecting the sense lines directly at the female connector.

To ensure correct operation, both sense lines (S+, S–) should be connected to their respective power outputs (Vo1+ and Vo1–), and the voltage difference between any sense line and its respective power output (as measured on the connector) should not exceed the following values:

Table 9: Maximum voltage compensation allowed using sense lines

Output voltage	Total voltage difference between sense lines and their respective outputs	Voltage difference between Vo– and S–
5.1 V	<0.5 V	<0.25 V
12 V, 15 V, 24 V	<1.0 V	<0.25 V

Note: If the output voltages are increased above $V_{o\,nom}$ via R-input control, option P setting, remote sensing or option T, the output currents must be reduced accordingly, so that $P_{o\,nom}$ is not exceeded.

Programmable Output Voltage (R-Function)

As a standard feature, the converters offer an adjustable output voltage, identified by letter R in the type designation. The control input R (pin 16) accepts either a control voltage V_{ext} or a resistor R_{ext} to adjust the desired output voltage. When R is not connected, the output voltage is set to $V_{o\,nom}$.

a) Adjustment by means of an external control voltage V_{ext} between pin 16 (R) and pin 14:

The control voltage range is 0 – 2.75 VDC and allows an output voltage adjustment in the range of approximately 0 – 110% $V_{o\,nom}$.

$$V_{ext} \approx \frac{V_o}{V_{o\,nom}} \cdot 2.5\ V$$

b) Adjustment by means of an external resistor:

Depending upon the value of the required output voltage the resistor shall be connected

either: Between pin 16 and pin 14 ($V_o < V_{o\,nom}$) to achieve an output voltage adjustment range of approximately 0 – 100% $V_{o\,nom}$.

or: Between pin 16 and pin 12 ($V_o > V_{o\,nom}$) to achieve an output voltage adjustment range of 100 – 110% $V_{o\,nom}$.

Warning:

- V_{ext} shall never exceed 2.75 VDC.
- The value of R'_{ext} shall never be less than the lowest value as indicated in table R'_{ext} (for $V_0 > V_{0\,nom}$) to avoid damage to the converter!

Notes:

- The R-Function excludes option P (output voltage adjustment by potentiometer).

  If the output voltages are increased above $V_{o\,nom}$ via R-input control, option P setting, remote sensing, or option T, the output currents should be reduced, so that $P_{o\,nom}$ is not exceeded.
- With double-output models the second output follows the value of the controlled main output.
- In case of parallel connection the output voltages should be individually set within a tolerance of 1 – 2%.

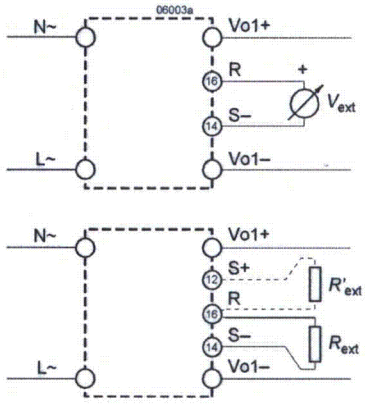


Fig. 21
Output voltage control for single-output models

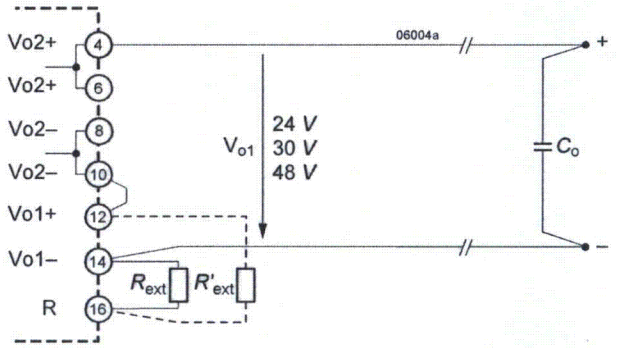


Fig. 22
Double-output models:
Wiring of the R-input for output voltages 24 V, 30 V, or 48 V with both outputs in series. A ceramic capacitor (C_o) across the load reduces ripple and spikes.

Test Jacks

Test jacks (pin diameter 2 mm) for measuring the main output voltage V_o or V_{o1} are located at the front of the converter. The positive test jack is protected by a series resistor (see: *Functional Description, block diagrams*).

The voltage measured at the test jacks is slightly lower than the value at the output terminals.

Table 10: R_{ext} for $V_o < V_{o\,nom}$; approximate values ($V_{i\,nom}$, $I_{o\,nom}$, series E 96 resistors); R'_{ext} = not fitted

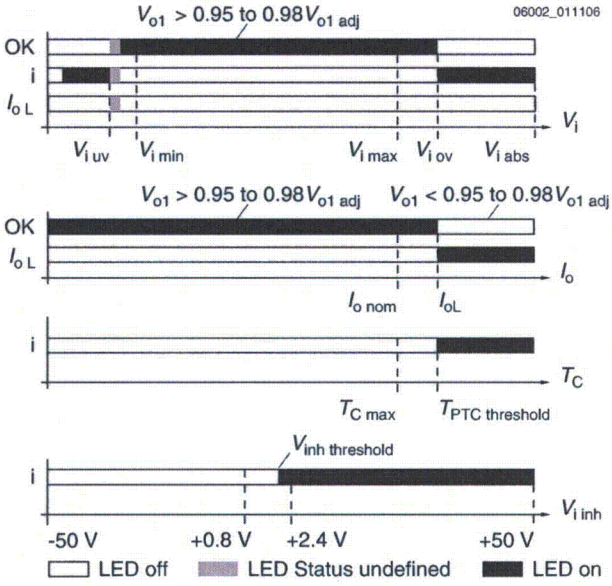
$V_{o\,nom}$ = 5.1 V		$V_{o\,nom}$ = 12 V			$V_{o\,nom}$ = 15 V			$V_{o\,nom}$ = 24 V		
V_o [V]	R_{ext} [kΩ]	V_o [V] [1]		R_{ext} [kΩ]	V_o [V] [1]		R_{ext} [kΩ]	V_o [V] [1]		R_{ext} [kΩ]
0.5	0.432	2	4	0.806	2	4	0.619	4	8	0.806
1.0	0.976	3	6	1.33	4	8	1.47	6	12	1.33
1.5	1.65	4	8	2	6	12	2.67	8	16	2
2.0	2.61	5	10	2.87	8	16	4.53	10	20	2.87
2.5	3.83	6	12	4.02	9	18	6.04	12	24	4.02
3.0	5.76	7	14	5.62	10	20	8.06	14	28	5.62
3.5	8.66	8	16	8.06	11	22	11	16	32	8.06
4.0	14.7	9	18	12.1	12	24	16.2	18	36	12.1
4.5	30.1	10	20	20	13	26	26.1	20	40	20
5.0	200	11	22	42.2	14	28	56.2	22	44	44.2

Table 10b: R'_{ext} for $V_o > V_{o\,nom}$; approximate values ($V_{i\,nom}$, $I_{o\,nom}$, series E 96 resistors); R_{ext} = not fitted

$V_{o\,nom}$ = 5.1 V		$V_{o\,nom}$ = 12 V			$V_{o\,nom}$ = 15 V			$V_{o\,nom}$ = 24 V		
V_o [V]	R'_{ext} [kΩ]	V_o [V] [1]		R'_{ext} [kΩ]	V_o [V] [1]		R'_{ext} [kΩ]	V_o [V] [1]		R'_{ext} [kΩ]
5.15	432	12.1	24.2	1820	15.2	30.4	1500	24.25	48.5	3320
5.2	215	12.2	24.4	931	15.4	30.8	768	24.5	49.0	1690
5.25	147	12.3	24.6	619	15.6	31.2	523	24.75	49.5	1130
5.3	110	12.4	24.8	475	15.8	31.6	392	25.0	50.0	845
5.35	88.7	12.5	25.0	383	16.0	32.0	316	25.25	50.5	698
5.4	75	12.6	25.2	316	16.2	32.4	267	25.5	51.0	590
5.45	64.9	12.7	25.4	274	16.4	32.8	232	25.75	51.5	511
5.5	57.6	12.8	25.6	243	16.5	33.0	221	26.0	52.0	442
		13.0	26.0	196				26.25	52.5	402
		13.2	26.4	169				26.4	52.8	383

[1] First column: V_o or V_{o1}; second column: double-output models with outputs in series connection

Display Status of LEDs



LEDs "OK", "i" and "$I_{o\,L}$" status versus input voltage
Conditions: $I_o \le I_{o\,nom}$, $T_C \le T_{C\,max}$, $V_{inh} \le 0.8$ V
$V_{i\,uv}$ = undervoltage lock-out, $V_{i\,ov}$ = overvoltage lock-out

LEDs "OK" and "$I_{o\,L}$" status versus output current
Conditions: $V_{i\,min} - V_{i\,max}$, $T_C \le T_{C\,max}$, $V_{inh} \le 0.8$ V

LED "i" versus case temperature
Conditions: $V_{i\,min} - V_{i\,max}$, $I_o \le I_{o\,nom}$, $V_{inh} \le 0.8$ V

LED "i" versus V_{inh}
Conditions: $V_{i\,min} - V_{i\,max}$, $I_o \le I_{o\,nom}$, $T_C \le T_{C\,max}$

Fig. 23
LED indicators

Battery Charging / Temperature Sensor

All converters with an R-input are suitable for battery charger applications, but we recommend to choose the models especially designed for this application, see *Model Selection*, table 2.

For optimal battery charging and life expectancy of the battery an external temperature sensor can be connected to the R-input. The sensor is mounted as close as possible to the battery and adjusts the output voltage according to the battery temperature.

Depending upon cell voltage and the temperature coefficient of the battery, different sensor types are available, see: *Accessories*.

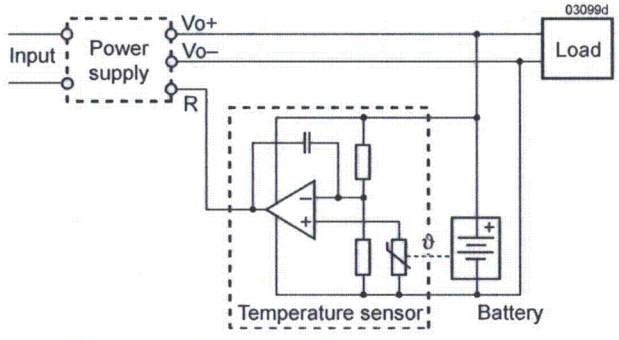


Fig. 24
Connection of a temperature sensor

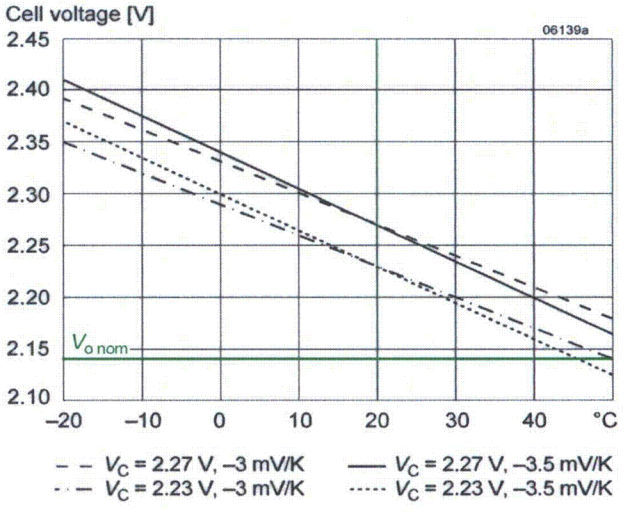


Fig. 25
Trickle charge voltage versus temperature for defined temperature coefficient. $V_{o\,nom}$ is the output voltage with open R-input.

Electromagnetic Compatibility (EMC)

A metal oxide VDR together with an input fuse and an input filter form an effective protection against high input transient voltages, which typically occur in most installations. The converters have been successfully tested to the following specifications:

Electromagnetic Immunity

Table 11: Electromagnetic immunity (type tests)

Phenomenon	Standard	Level	Coupling mode [1]	Value applied	Waveform	Source imped.	Test procedure	In oper.	Per-form. [2]
Electrostatic discharge (to case)	IEC/EN 61000-4-2	4	contact discharge	8000 V_p	1/50 ns	330 Ω	10 positive and 10 negative discharges	yes	A
			air discharge	15000 V_p					
Electromagnetic field	IEC/EN 61000-4-3	3	antenna	10 V/m	AM 80% 1 kHz	n.a.	80 – 1000 MHz	yes	A
				10 V/m	50% duty cycle, 200 Hz repetition frequency	n.a.	900 ±5 MHz	yes	A
Electrical fast transients/burst	IEC/EN 61000-4-4	4	capacitive, o/c	2000 V_p	bursts of 5/50 ns 2.5/5 kHz over 15 ms; burst period: 300 ms	50 Ω	60 s positive 60 s negative transients per coupling mode	yes	A
			i/c, +i/–i direct	4000 V_p					
Surges	IEC/EN 61000-4-5	3	i/c	2000 V_p	1.2/50 µs	12 Ω	5 pos. and 5 neg. surges per coupling mode	yes	A[3]
		4	+i/–i	2000 V_p		2 Ω			
Conducted disturbances	IEC/EN 61000-4-6	3	i, o, signal wires	10 VAC (140 dBµV)	AM 80% 1 kHz	150 Ω	0.15 – 80 MHz	yes	A
Voltage dips, short interruptions and variations	IEC/EN 6100-4-11	40%	+i/–i	230→92 →92	2→1→2 s	n.a.		yes	B[4]
		0%	+i/–i	230→0 →92					B[4]

[1] i = input, o = output, c = case
[2] A = Normal operation, no deviation from specifications, B = Normal operation, temporary loss of function or deviation from specs possible
[3] For converters with version V102 or higher. Older LKP models meet only B.
[4] Only LKP models have been tested.

Electromagnetic Emissions

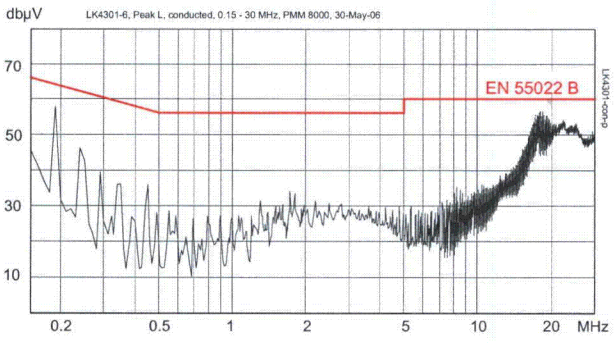


Fig. 26a
Conducted emissions (peak) at the phase input according to EN 55011/22, measured at $V_{i\,nom}$ and $I_{o\,nom}$ (LK4301-7R). The neutral line performs quite similar.

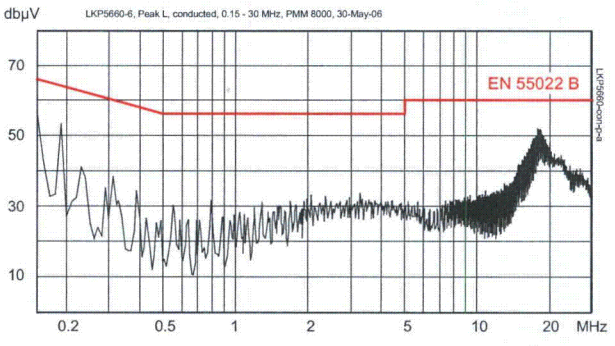


Fig. 26b
Conducted emissions (peak) at the phase input according to EN 55011/22, measured at $V_{i\,nom}$ and $I_{o\,nom}$ (LKP5660-7R). The neutral line performs quite similar.

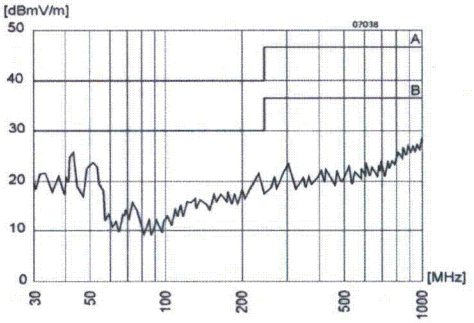


Fig. 27
Typical radiated emissions according to EN 55011/22, antenna 10 m distance, measured at $V_{i\ nom}$ and $I_{o\ nom}$.

Immunity to Environmental Conditions

Table 12: Mechanical and climatic stress

Test Method		Standard	Test Conditions		Status
Cab	Damp heat steady state	IEC/EN 60068-2-78:2001 MIL-STD-810D sect. 507.2	Temperature: Relative humidity: Duration:	40 $^{\pm 2}$ °C 93 $^{+2/-3}$ % 56 days	Converter not operating
Ea	Shock (half-sinusoidal)	IEC/EN 60068-2-27:1987 MIL-STD-810D sect. 516.3	Acceleration amplitude: Bump duration: Number of bumps:	100 g_n = 981 m/s^2 6 ms 18 (3 each direction)	Converter operating
Eb	Bump (half-sinusoidal)	IEC/EN 60068-2-29:1987 MIL-STD-810D sect. 516.3	Acceleration amplitude: Bump duration: Number of bumps:	40 g_n = 392 m/s^2 6 ms 6000 (1000 each direction)	Converter operating
Fc	Vibration (sinusoidal)	IEC/EN 60068-2-6:1995 MIL-STD-810D sect. 514.3	Acceleration amplitude: Frequency (1 Oct/min): Test duration:	0.35 mm (10 – 60 Hz) 5 g_n = 49 m/s^2 (60 – 2000 Hz) 10 – 2000 Hz 7.5 h (2.5 h each axis)	Converter operating
Fn	Random vibration broad band (digital control)	IEC/EN 60068-2-64	Acceleration spectral density: Frequency band: Acceleration magnitude: Test duration:	0.05 g_n^2/Hz 20 – 500 Hz 4.9 $g_{n\ rms}$ 3 h (1 h each axis)	Converter operating
Kb	Salt mist, cyclic (sodium chloride NaCl solution)	IEC/EN 60068-2-52:1996	Concentration: Duration: Storage: Storage duration: Number of cycles:	5% (30 °C) 2 h per cycle 40 °C, 93% rel. humidity 22 h per cycle 3	Converter not operating

[1] Set of DIN rail mounting brackets; see *Accessories*

Temperatures

Table 13: Temperature specifications, values given are for an air pressure of 800 – 1200 hPa (800 – 1200 mbar)

Temperature			-5		-6		-7		-9		
Characteristics		Conditions	min	max	min	max	min	max	min	max	Unit
T_A	Ambient temperature	Converter operating	–25[1]	50	–25[1]	60	–25	71	–40	71	°C
T_C	Case temperature [1]		–25[1]	85	–25[1]	90	–25	95	–40	95	
T_S	Storage temperature	Not operating	–40[2]	100	–40[2]	100	–40	100	–55	100	

[1] Minimum T_A and T_C for models with option E is –40 °C.
[2] Minimum T_S for models with option E is –55 °C.

Reliability

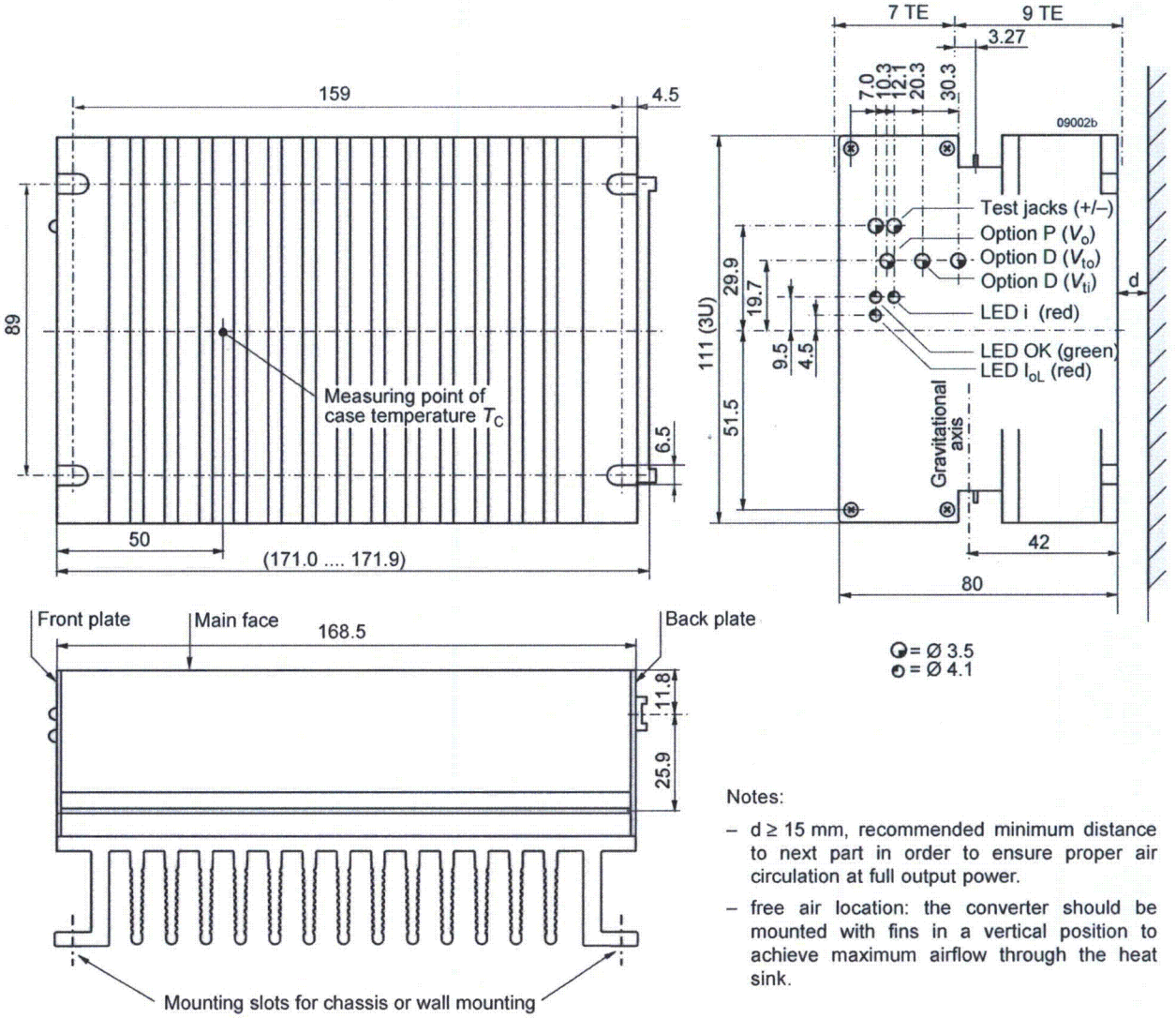
Table 14: MTBF calculated according to MIL-HDBK 217F

Values at specified case temperature	Model	Ground benign 40 °C	Ground fixed 40 °C	Ground fixed 70 °C	Ground mobile 50 °C	Unit
MTBF	LK4301-7ER	514 000	88 000	38 000	35 000	h

Mechanical Data

Dimensions in mm. The converters are designed to be inserted into a 19" rack, 160 mm long, according to IEC 60297-3.

European Projection



Notes:

- d ≥ 15 mm, recommended minimum distance to next part in order to ensure proper air circulation at full output power.
- free air location: the converter should be mounted with fins in a vertical position to achieve maximum airflow through the heat sink.

Fig. 28
Aluminium case K02 with heat sink, black finish, and self cooling; weight ≈ 1.55 kg

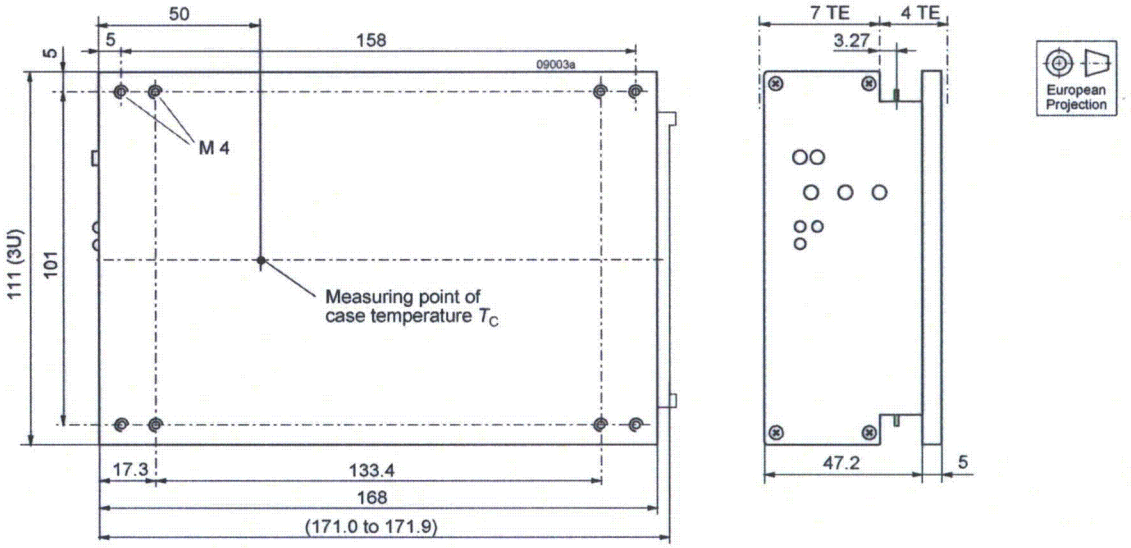


Fig. 29
Aluminium case K02 with option B1 (cooling plate), black finish and self cooling. Total weight ≈1.15 kg

Note: Long case with option B2, elongated by 60 mm for 220 mm rack depth, is available on request. (No LEDs, no test jacks.)

Safety and Installation Instructions

Connector Pin Allocation

The connector pin allocation table defines the electrical potentials and the physical pin positions on the H15 connector. The protective earth is connected by a leading pin (no. 24), ensuring that it makes contact with the female connector first.

Table 15: Pin allocation

Pin	Connector H15S2/S4[5]		Connector type H15			
no.	LK4003 (V_o = 5.1 V)		LK4000 (V_o ≥ 5.1 V)		LK/LKP5000	
4	Vo+	Positive output	Vo+	Positive output	Vo2+	Pos. output 2
6						
8	Vo–	Negative output	Vo–	Negative output	Vo2–	Neg. output 2
10						
12	S+	Sense+	S+	Sense+	Vo1+	Pos. output 1
14	S–	Sense–	S–	Sense–	Vo1–	Neg. output 1
16	R[1]	Control of V_o	R[1]	Control of V_o	R[1]	Control of V_{o1}
18	i	Inhibit	i	Inhibit	i	Inhibit
20	D[3]	Save data	D[3]	Save data	D[3]	Save data
	V[3]	ACFAIL				
22	T[4]	Current share	T[4]	Current share	T[4]	Current share
24[2]	⏚	Protective earth	⏚	Protective earth	⏚	Protective earth
26	N~	Neutral line	N~	Neutral line	N~	Neutral line
28						
30	L~	Phase line	L~	Phase line	L~	Phase line
32						

[1] Not connected, if option P is fitted.
[2] Leading pin (pre-connecting)
[3] Option D excludes option V and vice versa. Pin not connected, unless option D or V is fitted.
[4] Not connected, unless option T is fitted.
[5] Option K stands for the H15S4 connector (compatibility with LK1001)

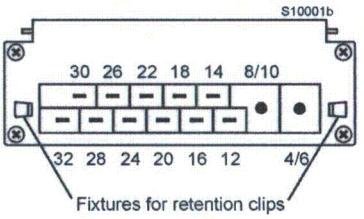


Fig. 30a
View of converter's male connector H15S2 (not for new designs)
Models with option K have a connector H15S4, where the contacts 26/28 and 30/32 are replaced by a high-current contact.

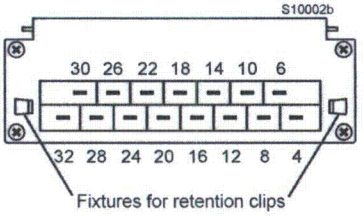


Fig. 30b
View of converter's male standard H15 connector

Installation Instructions

Note: These converters have a power factor correction (PFC). The LK4000/5000 models are intended to replace the LK1000 and LK2000 converters in order to comply with IEC/EN 61000-3-2. LK1000 is replaced by LK4003 with option K.

Switch off the system and check for hazardous voltages before altering any connection!

These converters are components, intended exclusively for inclusion within other equipment by an industrial assembly operation or by professional installers. Installation must strictly follow the national safety regulations in compliance with the enclosure, mounting, creepage, clearance, casualty, markings, and segregation requirements of the end-use application.

Connection to the system shall be made via the female connector H15 (standard) or H15S2; see: *Accessories*. Other installation methods may not meet the safety requirements.

Pin no. 24 (⏚) is reliably connected with the case. For safety reasons it is essential to connect this pin reliably to protective earth. See: *Safety of Operator-Accessible Output Circuits*.

The phase input 30/32 (L~) is connected via a built-in fuse (see: *Input Fuse* and table 4), which is designed to protect in the case of a converter failure.

An additional external fuse, suitable for the application, might be necessary in the wiring to the other line input 26/28 (N~) if:

- Local requirements demand an individual fuse in each source line
- Phase and neutral of the mains are not defined or cannot be assigned to the corresponding terminals (L~ to phase and N~ to neutral).
- Neutral and earth impedance is high or undefined

Notes:

- If the inhibit function is not used, pin no. 18 (i) should be connected to pin no. 14 (S–/Vo1–) to enable the output(s).
- Do not open the converters, or warranty will be invalidated.
- Due to high current values, the converters provide two internally parallel contacts for certain paths (pins 4/6, 8/10, 26/28 and 30/32). It is recommended to connect load and supply to both female connector pins of each path in order to keep the voltage drop low and to not overstress the connector contacts with high currents.
- If the second output of double-output models is not used, connect it parallel with the main output.

Make sure that there is sufficient airflow available for convection cooling. This should be verified by measuring the case temperature, when the converter is installed and operated in the end-use application. See: *Thermal Considerations*.

Ensure that a converter failure (e.g., an internal short-circuit) does not result in a hazardous condition. See also: *Safety of Operator-Accessible Output Circuit*.

Standards and Approvals

The converters are approved according to UL 60950-1, CSA 60950-1, IEC 60950-1, and EN 60950-1.

The converters correspond to Class I equipment and have been evaluated for:

- Building-in
- Basic insulation between input and case based on 250 VAC, and double or reinforced insulation between input and output(s).
- Basic insulation between output(s) and case based on 200 VAC.
- Functional insulation between outputs.
- Overvoltage category II
- Pollution degree 2 environment
- Max. altitude: 2000 m.
- The converters fulfill the requirements of a fire enclosure.

CB-scheme is available: SI-1819 (IEC 60950-1:2001)

All boards and components of the converters are coated with a protective lacquer.

The converters are subject to manufacturing surveillance in accordance with the above mentioned UL standards and ISO 9001:2000.

Cleaning Agents

In order to avoid possible damage, any penetration of cleaning fluids is to be prevented, since the power supplies are not hermetically sealed.

Protection Degree

Condition: Female connector fitted to the unit.

- IP 30: All models except those with option P, and except those with option D or V including a potentiometer.
- IP 20: All models fitted with option P, or with option D or V with potentiometer.

Leakage Currents

Leakage currents flow due to internal leakage capacitances and Y-capacitors. The current values are proportional to the supply voltage and are specified in the table below.

Table 16: Leakage currents

Characteristic		Class I	Unit
Maximum earth leakage current	Permissible according to IEC/EN 60950	3.5	mA
	Typ value at 254 V, 50 Hz (LK models)	0.8	
	Typ value at 254 V, 50 Hz (LKP models)	0.8	

Isolation

The electric strength test is performed in the factory as routine test in accordance with EN 50116 and IEC/EN 60950 and should not be repeated in the field. Power-One

Table 17: Isolation

Characteristic		Input to case and output(s)	Output(s) to case	Output 1 to output 2	Unit
Electric strength test	Factory test >1 s	2.8 [1]	1.4	0.15	kVDC
	AC test voltage equivalent to factory test	2.0	1.0	0.1	kVAC
Insulation resistance at 500 VDC		>300	>300	>100 [2]	MΩ
Creapage distances		≥3.2 [3]	--	--	mm

[1] According to EN 50116 and IEC/EN 60950, subassemblies connecting input to output are pre-tested with 5.6 kVDC or 4 kVAC.
[2] Tested at 150 VDC
[3] Input to outputs: 6.4 mm

will not honor any warranty claims resulting from electric strength field tests.

Safety of Operator-Accessible Output Circuits

If the output circuit of a converter is operator-accessible, it shall be an SELV circuit according to IEC/EN 60950.

The table below shows a possible installation configuration, compliance with which causes the output circuit of a K Series AC-DC converter to be a SELV circuit according to IEC/EN 60950 up to a configured output voltage of 36 V (sum of nominal voltages connected in series) .

However, it is the sole responsibility of the installer to ensure compliance with the applicable safety regulations.

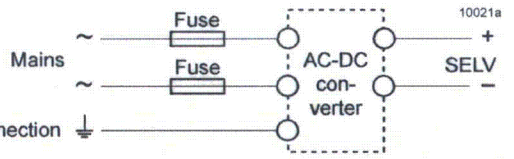


Fig. 31
Schematic safety concept.

Table 18: Safety concept leading to a SELV output circuit

Conditions	AC-DC converter	Installation	Result
Nominal voltage	Grade of insulation between input and output provided by the AC-DC converter	Measures to achieve the resulting safety status of the output circuit	Safety status of the AC-DC converter output circuit
Mains ≤250 VAC	Double or reinforced	Earthed case[1] and installation according to the applicable standards	SELV circuit

[1] The earth connection has to be provided by the installer according to the relevant safety standards, e.g. IEC/EN 60950.

Description of Options

Table 19: Survey of options

Option	Function of option	Characteristic
-9	Extended operational ambient temperature range	T_A = –40 to 71 °C
E	Electronic inrush current limitation circuitry	Active inrush current limitation
P[2]	Potentiometer for fine adjustment of output voltage	Adjustment range +10/–60% of $V_{o\,nom}$, excludes R input
D[1]	Input and/or output undervoltage monitoring circuitry	Safe data signal output (D0 – DD)
V[1]	Input and/or output undervoltage monitoring circuitry	ACFAIL signal according to VME specifications (V0, V2, V3)
T	Current sharing	Interconnect T-pins if paralleling outputs (max 5 converters)
K	H15S4 connector for 5.1 V output models	For new designs; provides compatibility with LK1001 models
B1, B2	Cooling plate (160 or 220 mm long)	Replaces standard heat sink, allowing direct chassis-mounting

[1] Option D excludes option V and vice versa; option V only for 5.1 V outputs.
[2] Option P is not available for battery charger models.

-9 Extended Temperature Range

Option -9 extends the operational ambient temperature range from –25 to 71 °C (standard) to –40 to 71 °C. The power supplies provide full nominal output power with convection cooling. Option -9 excludes inrush current limitation by NTC.

E Inrush Current Limitation

The converters may be supplemented by an electronic circuit replacing the standard built-in NTC to achieve an enhanced inrush current limiting function.

Note: Subsequent switch-on cycles at start-up are limited to max. 10 cycles during the first 20 seconds (cold converter) and then to max. 1 cycle every 8 s.

Table 20: Inrush current characteristics with option E

Characteristics V_i = 230 VAC		all models typ	max	Unit
$I_{inr\,p}$	Peak inrush current	–	25.3	A
t_{inr}	Inrush current duration	35	50	ms

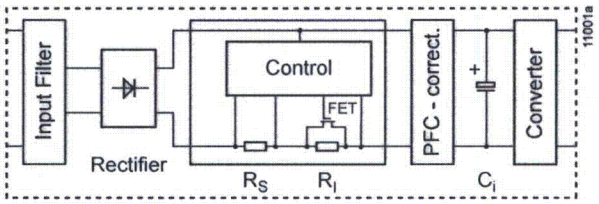


Fig. 32
Option E block diagram

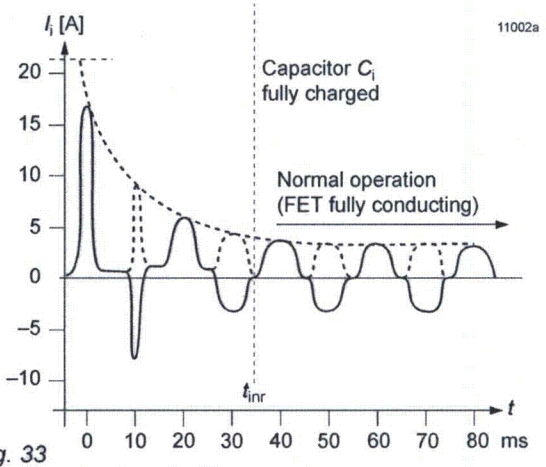


Fig. 33
Typ. inrush current with option E
V_i = 230 VAC, f_i = 50 Hz, $P_o = P_{o\,nom}$

P Potentiometer

A potentiometer provides an output voltage adjustment range of +10/–60% of $V_{o\,nom}$. It is accessible through a hole in the front cover. Option P is not available for battery charger models and is not recommended for converters connected in parallel.

Option P excludes the R-function. With double output units both outputs are influenced by the potentiometer setting (doubling the voltage, if the outputs are in series).

If the output voltages are increased above $V_{o\,nom}$ via R input control, option P setting, remote sensing or option T, the output current(s) should be reduced accordingly, so that $P_{o\,nom}$ is not exceeded.

T Current Sharing

This option ensures that the output currents are approximately shared between all parallel-connected converters, hence increasing system reliability. To use this facility, simply interconnect the T pins of all converters and make sure that the reference for the T signal, pin 14 (S– or the Vo1–), are also connected together. The load lines should have equal length and cross section to ensure equal voltage drops.

Not more than 5 converters should be connected in parallel. The R pins should be left open-circuit. If not, the output voltages must be individually adjusted prior to paralleling within 1 to 2% or the R pins should be connected together.

Parallel connection of converters with option P is not recommended.

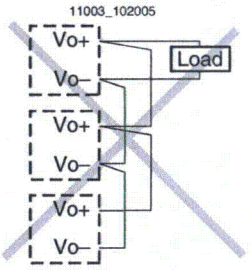
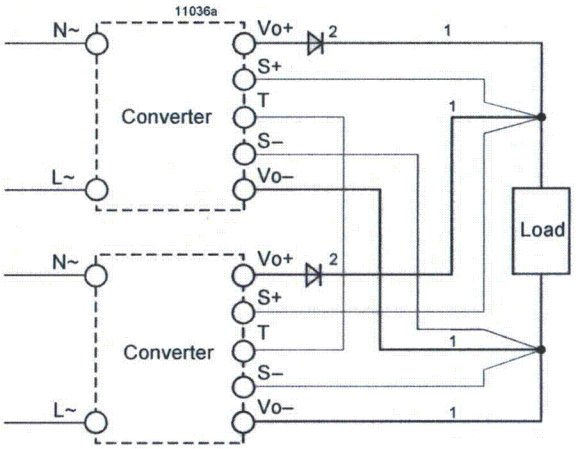


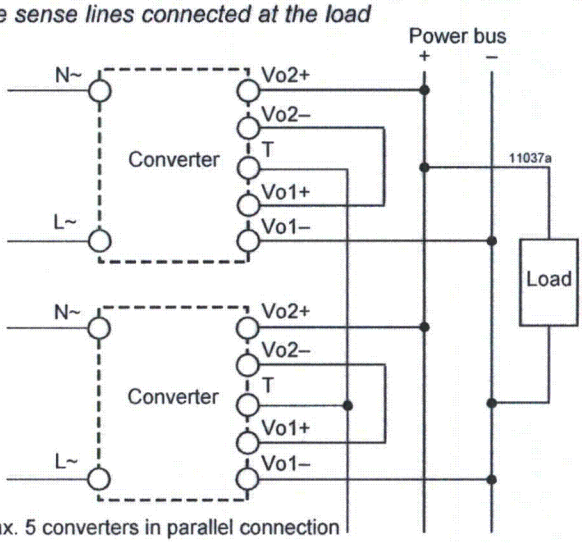
Fig. 34
Example of poor wiring for connection in parallel



Max. 5 converters in parallel connection

[1] Lead lines should have equal length and cross section, and should run in the same cable loom.
[2] Diodes recommended in redundant operation only

Fig. 35
Paralleling of single-output models using option T with the sense lines connected at the load



Max. 5 converters in parallel connection

Fig. 36
Paralleling of double-output models with the outputs connected in series, and using option T with power bus. The signal at the T pins is referenced to Vo1–.

D Undervoltage Monitor

The input and/or output undervoltage monitoring circuit operates independently of the built-in input undervoltage lockout circuit. A logic "low" (JFET output) or "high" signal (NPN output) is generated at the D output (pin 20), when one of the monitored voltages drops below the preselected threshold level V_t. This signal is referenced to Vo–/Vo1–. The D output recovers, when the monitored voltages exceed $V_t + V_h$. The threshold level V_{bi} is adjusted in the factory. The threshold level V_{to} is either adjusted by a potentiometer, accessible through a hole in the front cover, or adjusted in the factory to a fixed value specified by the customer.

Option D exists in various versions D0 – DD, as shown in the table below.

Table 21: Undervoltage monitoring functions

Output type JFET	Output type NPN	Monitoring V_b [4]	Monitoring V_{o1}	Minimum adjustment range of threshold level V_t V_{tb} [4]	Minimum adjustment range of threshold level V_t V_{to}	Typical hysteresis V_{ho} [% of V_t] for $V_{t\,min} - V_{t\,max}$ V_{ho}
D1	D5	no	yes	-	3.5 – 40 V [1]	2.5 – 0.6
D2	D6	yes	no	355 VDC	-	-
D3	D7	yes	yes	355 VDC	(0.95 – 0.985 V_{o1}) [2]	"0"
D4	D8	no	yes	-	(0.95 – 0.985 V_{o1}) [2]	"0"
D0	D9	no	yes	-	3.5 – 40 V [3]	2.5 – 0.6
		yes	yes	355 VDC	3.5 – 40 V [3]	2.5 – 0.6
	DD	yes	yes	355 VDC	3.5 – 40 V [1]	2.5 – 0.6

[1] Threshold level adjustable by potentiometer
[2] Fixed value. Tracking if V_{o1} is adjusted via R-input, option P or sense lines.
[3] The threshold level permanently adjusted according to customer specification ±2% at 25 °C. Any value within the specified range is basically possible, but causes a special type designation in addition to the standard option designations (D0/D9).
[4] V_b is the voltage generated by the boost regulator. When V_b drops below 355 V, the D signal triggers, and the output(s) will remain powered during nearly the full hold-up time t_h.

JFET output (D0 – D4):

Pin D is internally connected via the drain-source path of a JFET (self-conducting type) to the negative potential of output 1. $V_D \leq 0.4$ V (logic low) corresponds to a monitored voltage level (V_i and/or V_{o1}) $< V_t$. The current I_D through the JFET should not exceed 2.5 mA. The JFET is protected by a 0.5 W Zener diode of 8.2 V against external overvoltages.

V_b, V_{o1} status	D output, V_D
V_b or $V_{o1} < V_t$	low, L, $V_D \leq 0.4$ V at $I_D = 2.5$ mA
V_b and $V_{o1} > V_t + V_h$	high, H, $I_D \leq 25$ µA at $V_D = 5.25$ V

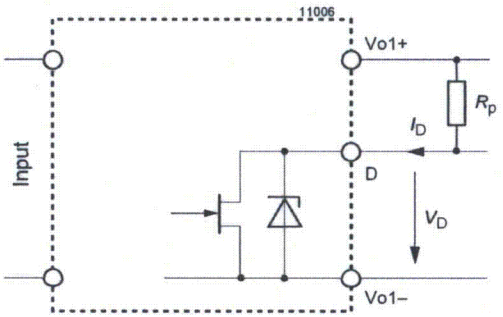


Fig. 37
Option D0 – D4: JFET output, $I_D \leq 2.5$ mA

NPN output (D5 – DD):

Pin D is internally connected via the collector-emitter path of a NPN transistor to the negative potential of output 1. $V_D < 0.4$ V (logic low) corresponds to a monitored voltage level (V_i and/or V_{o1}) $> V_t + V_h$. The current I_D through the open collector should not exceed 20 mA. The NPN output is not protected against external overvoltages. V_D should not exceed 40 V.

V_b, V_{o1} status	D output, V_D
V_b or $V_{o1} < V_t$	high, H, $I_D \leq 25$ µA at $V_D = 40$ V
V_b and $V_{o1} > V_t + V_h$	low, L, $V_D \leq 0.4$ V at $I_D = 20$ mA

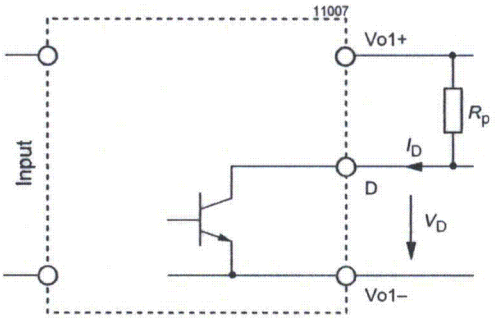
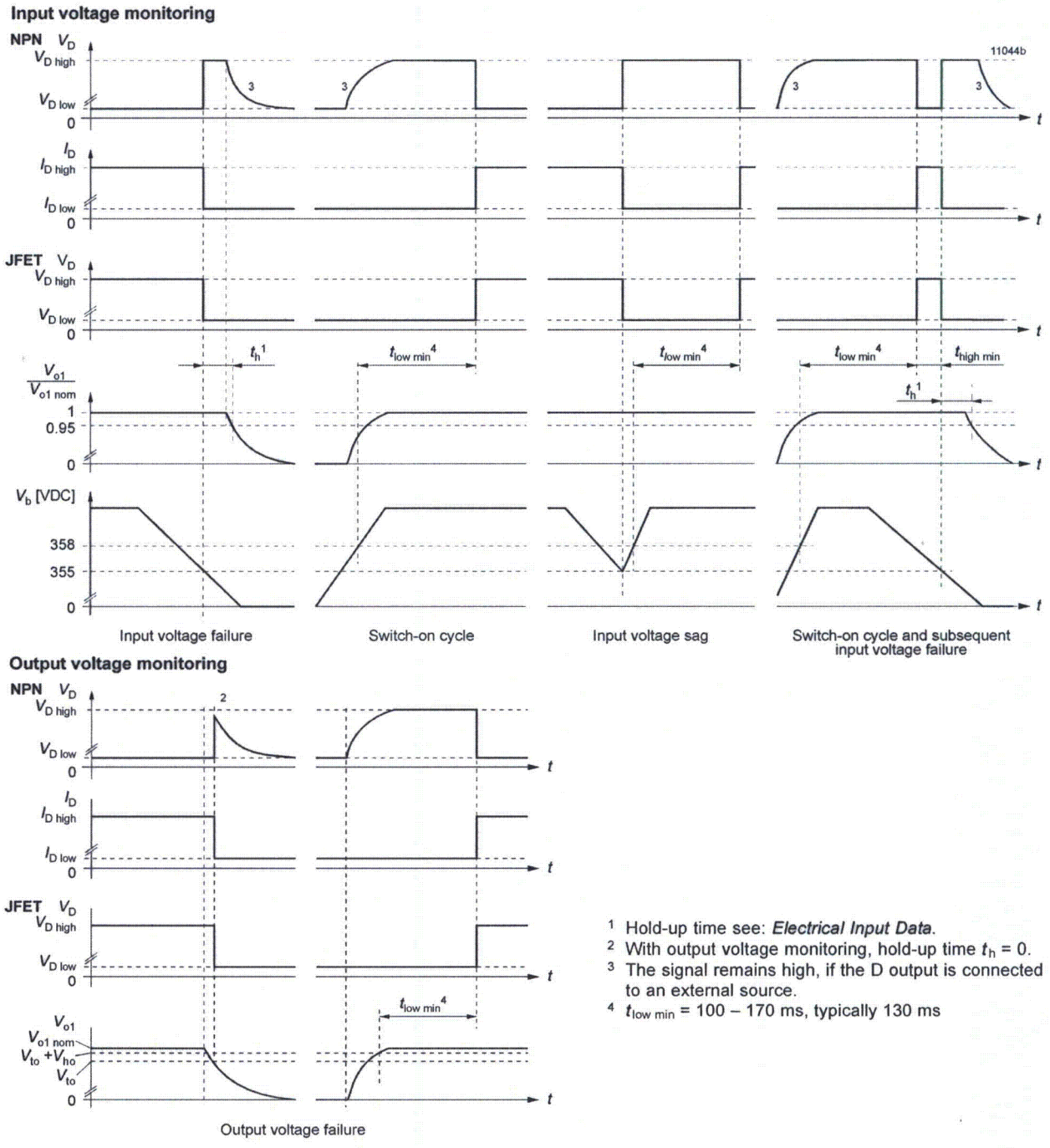


Fig. 38
Option D5 – DD: NPN output, $V_{o1} \leq 40$ V, $I_D \leq 20$ mA

Table 22: D-output logic signals

Version of D	$V_b < V_t$ resp. $V_o < V_t$	$V_b > V_t + V_h$ resp. $V_o > V_t$	Configuration
D1, D2, D3, D4, D0	low	high	JFET
D5, D6, D7, D8, D9, DD	high	low	NPN



1 Hold-up time see: ***Electrical Input Data***.
2 With output voltage monitoring, hold-up time $t_h = 0$.
3 The signal remains high, if the D output is connected to an external source.
4 $t_{low\,min}$ = 100 – 170 ms, typically 130 ms

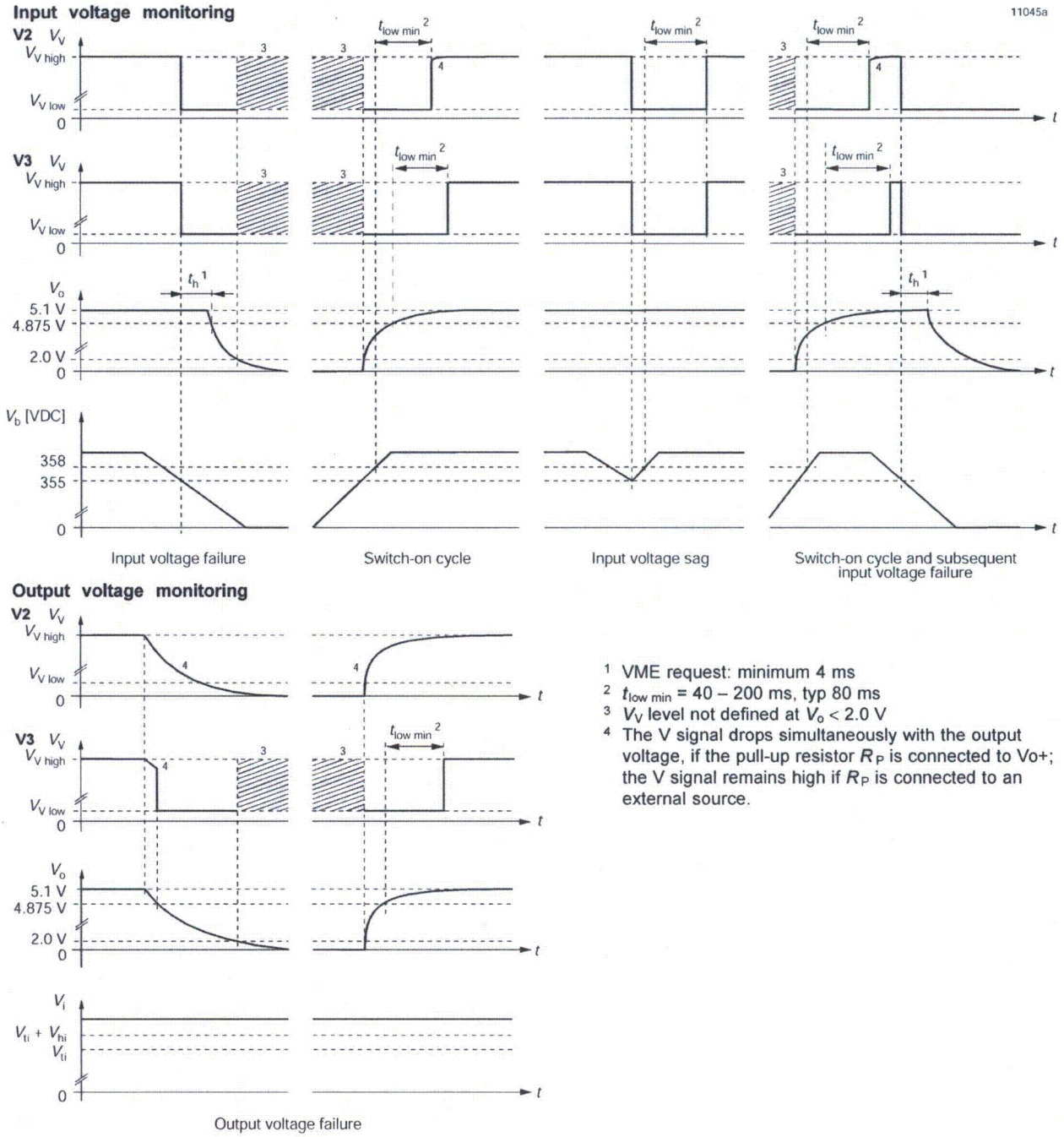
Fig. 39
Relationship between V_b, V_{o1}, V_D, $V_{o1}/V_{o1\,nom}$ versus time

V ACFAIL Signal (VME)

Available only for models with V_o = 5.1 V.

This option defines an undervoltage monitoring circuit for the input and main output voltage. It generates the ACFAIL signal (V signal) according to the VME standard.

The low state level of the ACFAIL signal is specified at a sink current of $I_V \leq 48$ mA to $V_V \leq 0.6$ V (open-collector output of an NPN transistor). The pull-up resistor feeding the open-collector output should be placed on the VME backplane.



1 VME request: minimum 4 ms
2 $t_{low\,min}$ = 40 – 200 ms, typ 80 ms
3 V_V level not defined at V_o < 2.0 V
4 The V signal drops simultaneously with the output voltage, if the pull-up resistor R_P is connected to Vo+; the V signal remains high if R_P is connected to an external source.

Fig. 40
V_{cb}, V_o, V_V, I_V, $V_o/V_{o\,nom}$ versus time.

After the ACFAIL signal has gone low, the VME standard requires a hold-up time t_h of at least 4 ms before the 5.1 V output drops at full load to 4.875 V. This hold-up time t_h is provided by the capacitance supporting the boost voltage V_b. See: *Hold-up Time*.

Table 23: Undervoltage monitor functions

V output (VME compatible)	Monitoring V_b	Monitoring V_{o1}	Minimum adjustment range of threshold level V_{tb}	Minimum adjustment range of threshold level V_{to}
V2	yes	no	355 VDC [1]	-
V3	yes	yes	355 VDC [1]	0.95 – 0.985 V_{o1} [2]

[1] Option V monitors the boost regulator output voltage. The trigger level is adjusted in the factory to 355 VDC.
[2] Fixed value between 95% and 98.5% of V_{o1}

Option V operates independently of the built-in input undervoltage lockout circuit. A logic "low" signal is generated at pin 20 as soon as one of the monitored voltages drops below the preselected threshold level V_t. The return for this signal is Vo–. The V output recovers, when the monitored voltage(s) exceed(s) $V_t + V_h$. The threshold level V_{tb} is adjusted in the factory to 355 VDC. The threshold level V_{to} is adjusted in the factory to a customer-specified value.

V-output (V2, V3):

Connector pin V is internally connected to the open collector of an NPN transistor. The emitter is connected to the negative potential of the main output. $V_V \leq 0.6$ V (logic low) corresponds to a monitored voltage level (V_i and/or V_o) $< V_t$. The current I_V through the open collector should not exceed 50 mA. The NPN output is not protected against external overvoltages. V_V should not exceed 60 V.

Table 24: Status of V output

V_b, V_o status	V output, V_V
V_b or $V_o < V_t$	low, L, $V_V \leq 0.6$ V at $I_V = 50$ mA
V_b and $V_{o1} > V_t + V_h$	high, H, $I_V \leq 25$ µA at $V_V = 5.1$ V

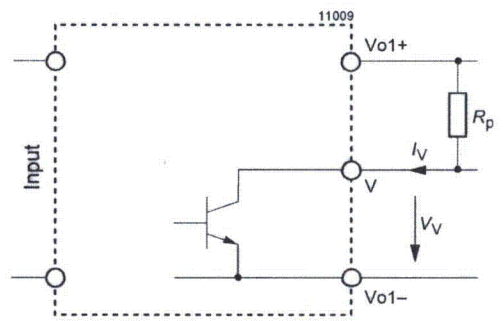


Fig. 41
Output configuration of options V2 and V3

K Connector H15S4

Models with 5.1 V output are fitted with a connector H15S4 (rather than H15S2). This option should be used for new designs and provides compatibility to LK1001 models.

B1 Cooling Plate (see: *Mechanical Data*)

Where a cooling surface is available, we recommend the use of a cooling plate (option B1) instead of the standard heat sink. The mounting system should ensure sufficient cooling capacity to guarantee that the maximum case temperature $T_{C\ max}$ is not exceeded. The cooling capacity is calculated by:

$$P_{Loss} = \frac{(100\% - \eta)}{\eta} \cdot V_o \cdot I_o$$

Efficiency η see: *Model Selection*

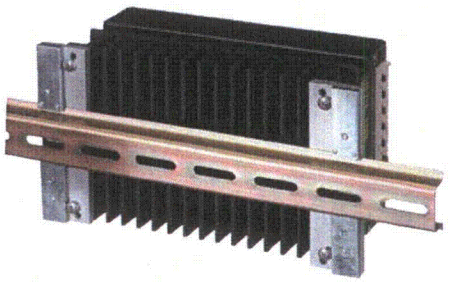
Elongated case for 220 mm rack depth need: **Option B2.**

Accessories

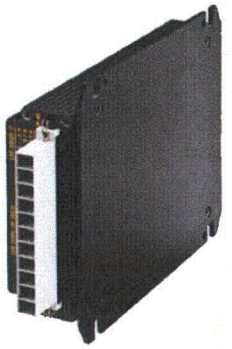
A variety of electrical and mechanical accessories are available including:

- Front panels for 19" rack: Schroff 16 TE /3U [HZZ00831] and 16 TE /6U [HZZ00832], or Intermas 16 TE /3U [HZZ00731]
- Mating H15 connectors with screw, solder, fast-on or press-fit terminals.
- Cable connector housing: Screw version [HZZ00141] or retention clip version [HZZ00142]
- Connector retention clips (2x) [HZZ01209]
- Connector retention brackets CRB [HZZ01216]
- Coding clips for connector coding [HZZ00202]
- DIN-rail mounting assembly DMB-K/S [HZZ0615]
- Wall-mounting plate K02 [HZZ01213] for models with option B1
- Additional external input and output filters
- Battery sensor [S-KSMH...] for using the converter as a battery charger. Different cell characteristics can be selected. See: *Battery Charging/Temperature Sensor*

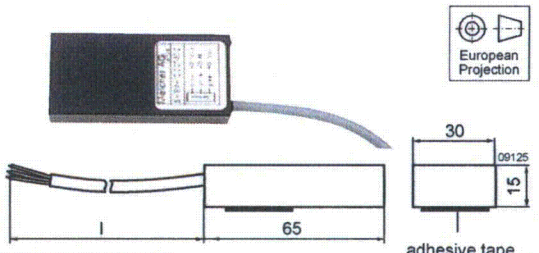
For additional accessory product information, see the accessory data sheets listed with each product series or individually at *www.power-one.com* through the following menus: "Select Products", "Select Data Sheets & Application Notes".



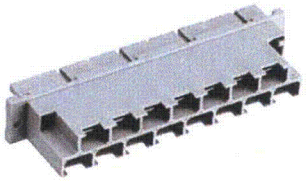
DIN-rail mounting assembly DMB-K/S



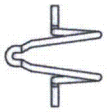
Wall-mounting plate MOUNTINGPLATE-K02



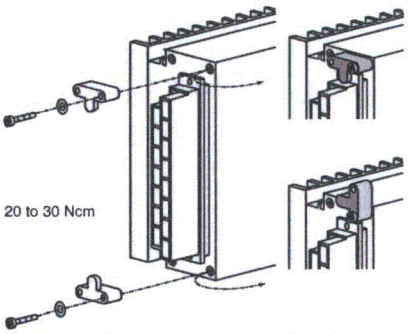
Battery temperature sensor



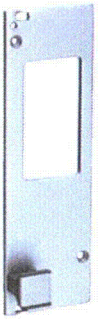
H15 female connector, code key system



Connector retention clip



Connector retention bracket CRB



Different front panels

EC Declaration of Conformity

We

Power-One AG
Ackerstrasse 56, CH-8610 Uster

declare under our sole responsibility that all K and S Series AC-DC and DC-DC converters carrying the CE-mark are in conformity with the provisions of the Low Voltage Directive (LVD) 73/23/EEC of the European Communities.

Conformity with the directive is presumed by conformity with the following harmonized standards:

- EN 61204:1995 (= IEC 61204:1993, modified)
  Low-voltage power supply devices, DC output - Performance characteristics and safety requirements

- EN 60950-1:2003 (IEC 60950-1:2005)
  Safety of information technology equipment.

The installation instructions given in the corresponding data sheet describe correct installation leading to the presumption of conformity of the end product with the LVD. All K and S Series AC-DC and DC-DC converters are components, intended exclusively for inclusion within other equipment by an industrial assembly operation or by professional installers. They must not be operated as stand alone products.

Hence conformity with the Electromagnetic Compatibility Directive 89/336/EEC (EMC Directive) needs not to be declared. Nevertheless, guidance is provided in most product application notes on how conformity of the end product with the indicated EMC standards under the responsibility of the installer can be achieved, from which conformity with the EMC directive can be presumed.

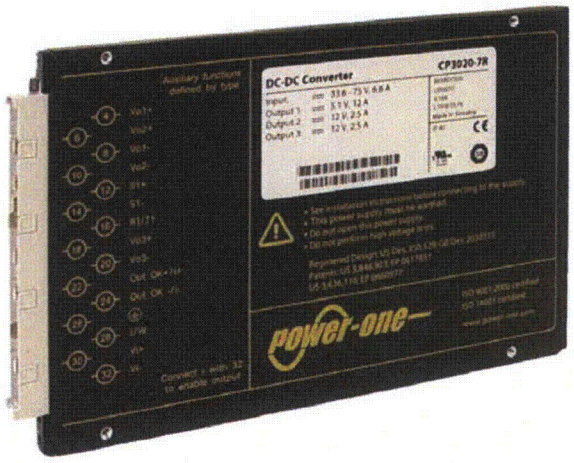
Uster, 9 October 2006 Power-One AG

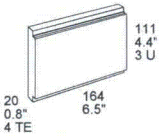
R. Baldauf

Rolf Baldauf
Vice President, Engineering

J. Milavec

Johann Milavec
Director Projects and IP





RoHS Compliant

Features

- RoHS lead-free-solder and lead-solder-exempted products available
- Wide input voltage ranges up to 150 VDC
- 1, 2, 3, or 4 isolated outputs up to 96 V
- Class I equipment
- Very high efficiency
- Extremely low inrush current, hot swappable
- Excellent surge and transient protection
- Many output configurations available with flexible load distribution
- Externally adjustable output voltage
- Inhibit primary or secondary referenced
- Redundant operation (n+1), sense lines, current sharing option
- Extremly slim case (4TE, 20 mm), fully enclosed
- Hipot test voltage 2.1 kVDC
- All PCBs coated with protective lacquer
- Telecom-compatible input voltage range of DP models according to ETS 300132-2
- CompactPCI-compatible output voltage (xP4720)

Safety according to IEC/EN 60950-1 and UL 60950-1

Description

These extremely compact DC-DC converters incorporate all necessary input and output filtering, signalling, and protection features, which are required in the majority of applications. The converters provide important advantages such as flexible output power through primary current limitation, extremely high efficiency, excellent reliability, very low ripple and RFI noise levels, full input-to-output isolation, negligible inrush current, soft start, overtemperature protection, and input over-/undervoltage lockout.

The converter inputs are protected against surges and transients occurring on the source lines and cover a total input voltage range from 16 to 150 VDC with five different types. The outputs are continuously open- and short-circuit proof.

Full system flexibility and n+1 redundant operating mode are possible due to series or parallel connection capabilities of the outputs under the specified conditions. When several converters are connected in parallel, the T option can be employed using a single wire connection between the converters to ensure good current sharing. LEDs at the front panel and an isolated output OK option indicate the status of the converter. Voltage suppressor diodes and an independent second control loop protect the outputs against an internally generated overvoltage.

The converters are designed using planar magnetics

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transformers and control circuits in hybrid technology. There are always two powertrains fitted to a converter, each consisting either of a single output with synchronous rectifier or of a controlled main output with a tracking second output. The output power may be flexibly distributed among the main and the tracking output of each powertrain. Close magnetic coupling in the transformers and output conductors together with circuit symmetry ensure tight tracking of the auxiliary output. The switching frequency is fixed.

As a modular power supply or as part of a distributed power supply system, the low-profile design significantly reduces the required volume without sacrificing high reliability. The converters are particularly suitable for 19" rack systems occupying 3U/4TE only, but they can also be chassis-mounted by means of four screws. Connector type is H15 (or H15S2 for some single-output models). The fully enclosed black-coated aluminium case acts as heat sink and RFI shield and protects the converter together with the coating of all components against environmental impacts.

Model Selection

Note: Only standard models are listed. Other configurations are possible as well; contact Power-One.

Table 1a: Model types BP, CP

Output 1, 4			Output 2, 3			Input voltage range and efficiency				Options
$V_{o\,nom}$ [V]	$P_{o\,nom}$ [W]	$P_{o\,max}$ [W]	$V_{o\,nom}$ [V]	$P_{o\,nom}$ [W]	$P_{o\,max}$ [W]	η [2] [%]	$V_{i\,min} - V_{i\,max}$ [4] 16–36 V	η [2] [%]	$V_{i\,min} - V_{i\,max}$ [4] 33.6–75 V	
3.3	100	132	-	-	-	86	BP1101-9R	86	CP1101-9R	-7
5.1	122	183	-	-	-	87	BP1001-9R	88	CP1001-9R	D
12	120	192	-	-	-	87.5	BP1301-9R	88.5	CP1301-9R	T[5]
15	120	194	-	-	-	88.5	BP1501-9R	88.5	CP1501-9R	i
24	120	192	-	-	-	88	BP1601-9R	89	CP1601-9R	K[8]
3.3	50	66	5.1	61	91	86	BP2101-9R	86	CP2101-9R	B1, B3
5.1	61	91	5.1	61	91	87	BP2001-9R	88	CP2001-9R	G
5.1	61	91	12	60	96	87	BP2020-9R	88	CP2020-9R	
12	60	96	12	60	96	87.5	BP2320-9R	88.5	CP2320-9R	
15	60	97	15	60	97	88.5	BP2540-9R	88.5	CP2540-9R	
24	60	96	24	60	96	88	BP2660-9R	89	CP2660-9R	
5.1	61	91	12, 12[3]	60[1]	96[1]	87	BP3020-9R	88	CP3020-9R	
5.1	61	91	15, 15[3]	60[1]	96[1]	87.5	BP3040-9R	88.5	CP3040-9R	
5.1	61	91	24, 24[3]	60[1]	96[1]	87.5	BP3060-9R	88.5	CP3060-9R	
5.1, 3.3[7]	30	50	12, 12[3]	60[1]	96[1]	-	BP4720-9R[6]	-	CP4720-9R[6]	-7
12, 12[3]	60[1]	96[1]	12, 12[3]	60[1]	96[1]	88	BP4320-9R	89	CP4320-9R	D, i
15, 15[3]	60[1]	96[1]	15, 15[3]	60[1]	96[1]	88	BP4540-9R	89	CP4540-9R	B1, B3
24, 24[3]	60[1]	96[1]	24, 24[3]	60[1]	96[1]	88	BP4660-9R	89	CP4660-9R	G

[1] The power of both outputs may in sum not exceed the total power for the specified ambient temperature.
[2] Min efficiency at $V_{i\,nom}$, $P_{o\,nom}$, T_A = 25 °C. Typical values are approx. 2% better.
[3] Isolated tracking output (±5% $V_{o\,nom}$, if each output is loaded with ≥ 5% of $P_{o\,nom}$). Parallel or series configuration possible
[4] Short deviations below $V_{i\,min}$ and beyond $V_{i\,max}$ according to EN 50155 possible
[5] Only available for outputs with 3.3 V or 5.1 V
[6] Compatible to CompactPCI® specification; for detailed specification contact Power-One.
[7] Outputs 5.1 and 3.3 V have a common return.
[8] H15 standard connector, rather then H15-S2 connector; applies for xP1101 and xP1001.

Table 1b: Model types DP, EP

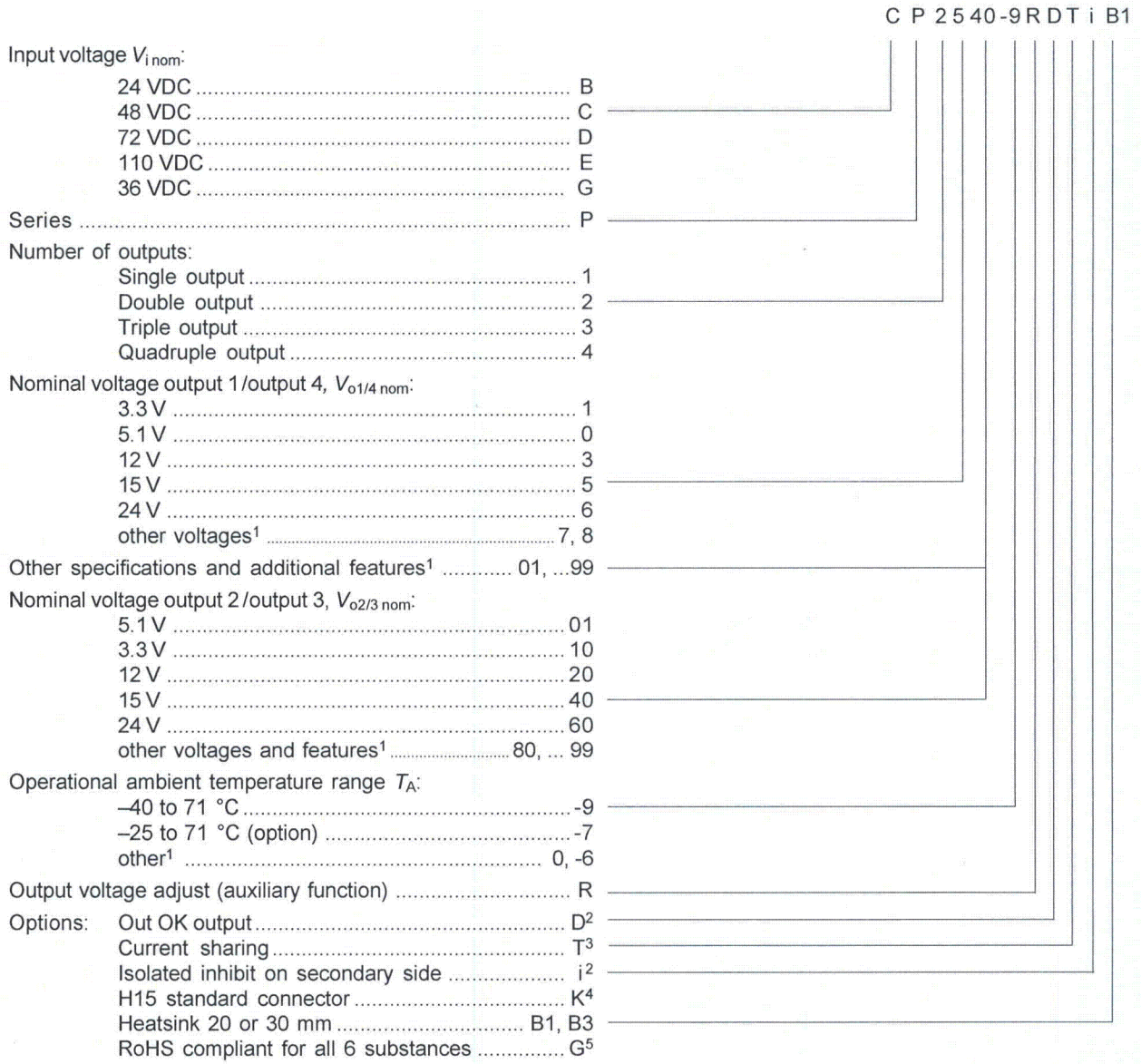
Output 1, 4			Output 2, 3			Input voltage range and efficiency[2]				Options
$V_{o\,nom}$ [V]	$P_{o\,nom}$ [W]	$P_{o\,max}$ [W]	$V_{o\,nom}$ [V]	$P_{o\,nom}$ [W]	$P_{o\,max}$ [W]	η[2] [%]	$V_{i\,min} - V_{i\,max}$[4] 40 – 100.8 V[9]	η[2] [%]	$V_{i\,min} - V_{i\,max}$[4] 66 – 150 V	
3.3	100	132	-	-	-	86	DP1101-9R	86	EP1101-9R	-7
5.1	122	183	-	-	-	88	DP1001-9R	88	EP1001-9R	D
12	120	192	-	-	-	88	DP1301-9R	87.5	EP1301-9R	T[5]
15	120	194	-	-	-	89	DP1501-9R	88	EP1501-9R	i
24	120	192	-	-	-	88.5	DP1601-9R	87.5	EP1601-9R	K[8]
3.3	50	66	5.1	61	91	86	DP2101-9R	86	EP2101-9R	B1, B3
5.1	61	91	5.1	61	91	88	DP2001-9R	88	EP2001-9R	G
5.1	61	91	12	60	96	88	DP2020-9R	87.5	EP2020-9R	
12	60	96	12	60	96	88	DP2320-9R	87.5	EP2320-9R	
15	60	97	15	60	97	89	DP2540-9R	88	EP2540-9R	
24	60	96	24	60	96	88.5	DP2660-9R	87.5	EP2660-9R	
5.1	61	91	12, 12[3]	60[1]	96[1]	87.5	DP3020-9R	87.5	EP3020-9R	
5.1	61	91	15, 15[3]	60[1]	96[1]	88	DP3040-9R	88	EP3040-9R	
5.1	61	91	24, 24[3]	60[1]	96[1]	88	DP3060-9R	88	EP3060-9R	
5.1, 3.3[7]	30	50	12, 12[3]	60[1]	96[1]	-	DP4720-9R[6]	-	EP4720-9R[6]	-7
12, 12[3]	60[1]	96[1]	12, 12[3]	60[1]	96[1]	89	DP4320-9R	88	EP4320-9R	D, i
15, 15[3]	60[1]	96[1]	15, 15[3]	60[1]	96[1]	89	DP4540-9R	88	EP4540-9R	B1, B1
24, 24[3]	60[1]	96[1]	24, 24[3]	60[1]	96[1]	89	DP4660-9R	87	EP4660-9R	G

Table 1c: Model types GP

Output 1, 4			Output 2, 3			Input voltage range and efficiency[2]		Options
$V_{o\,nom}$ [V]	$P_{o\,nom}$ [W]	$P_{o\,max}$ [W]	$V_{o\,nom}$ [V]	$P_{o\,nom}$ [W]	$P_{o\,max}$ [W]	η[2] [%]	$V_{i\,min} - V_{i\,max}$[4] 21.6 – 50.4 V	
3.3	100	132	-	-	-	86	GP1101-9R	-7
5.1	122	183	-	-	-	88	GP1001-9R	D
12	120	192	-	-	-	87.5	GP1301-9R	T[5]
15	120	194	-	-	-	88	GP1501-9R	i
24	120	192	-	-	-	87.5	GP1601-9R	K[8]
3.3	50	66	5.1	61	91	86	GP2101-9R	B1, B3
5.1	61	91	5.1	61	91	88	GP2001-9R	G
5.1	61	91	12	60	91	87.5	GP2020-9R	
12	60	96	12	60	96	87.5	GP2320-9R	
15	60	97	15	60	97	88	GP2540-9R	
24	60	96	24	60	96	87.5	GP2660-9R	
5.1	61	91	12, 12[3]	60[1]	96[1]	87.5	GP3020-9R	
5.1	61	91	15, 15[3]	60[1]	96[1]	88.5	GP3040-9R	
5.1	61	91	24, 24[3]	60[1]	96[1]	88.5	GP3060-9R	
5.1, 3.3[7]	30	50	12, 12[3]	60[1]	96[1]	-	GP4720-9R[6]	-7
12, 12[3]	60[1]	96[1]	12, 12[3]	60[1]	96[1]	88	GP4320-9R	D, i
15, 15[3]	60[1]	96[1]	15, 15[3]	60[1]	96[1]	88	GP4540-9R	B1, B3
24, 24[3]	60[1]	96[1]	24, 24[3]	60[1]	96[1]	88	GP4660-9R	G

1 The power of both outputs may in sum not exceed the total power for the specified ambient temperature.
2 Min efficiency at $V_{i\,nom}$, $P_{o\,nom}$, T_A = 25 °C. Typical values are approx. 2% better.
3 Isolated tracking output (±5% $V_{o\,nom}$, if each output is loaded with ≥ 5% of $P_{o\,nom}$). Parallel or series configuration possible
4 Short deviations below $V_{i\,min}$ and beyond $V_{i\,max}$ according to EN 50155 possible
5 Only available for outputs with 3.3 V or 5.1 V
6 Compatible to CompactPCI® specification; for detailed specification contact Power-One.
7 Outputs 5.1 and 3.3 V have a common return.
8 H15 standard connector, rather then H15-S2 connector; applies for xP1101 and xP1001.
9 According to ETS 300132-2 (DP models)

Part Number Description



[1] Customer-specific models.
[2] Option D and option i exclude each other.
[3] Only available for 3.3 V and 5 V outputs. Option T excludes option R, except for single-output models; refer to table 1.
[4] Only available for single-output models with 3.3 V or 5 V output
[5] G is always placed at the end of the part number. Consult Power-One for availability!

Example: CP 2540-9R: DC-DC converter, input voltage range 33.6 – 75 V, 2 regulated outputs each providing 15 V, equipped with R-control for output 1 and operating ambient temperature of –40 to 71 °C.

Note: All models exhibit the following auxiliary functions, which are not shown in the type designation: input and output filters, primary referenced inhibit, sense lines (single-, double- and triple-output models only), and LED indicators.

Product Marking

Basic type designation, applicable safety approval and recognition marks, CE mark, warnings, pin allocation, Power-One patents, company logo, specific type designation, input voltage range, nominal output voltage(s) and output current(s), degree of protection, batch no., serial no. and data code including production site, modification status and date of production. Identification of LEDs.

Output Configuration

The P Series allows high flexibility in output configuration to cover almost every individual requirement, by simply wiring outputs in parallel, in seriel, or in independent configuration, as shown in the following diagrams.

Parallel or serial operation of several converters with equal output voltage is possible, however it is not advantageous to connect converters in parallel without measures to provide reasonable current sharing. Choose suitable single-output models, if available.

Note: Unused tracking outputs should be connected parallel to the respective regulated outputs.

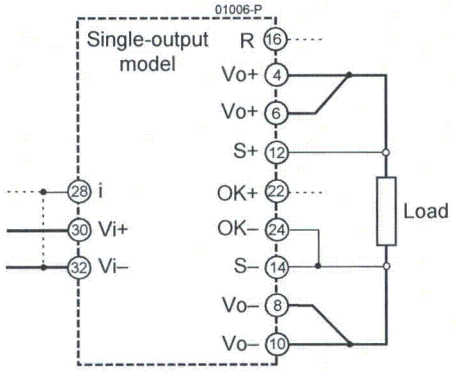


Fig. 1
Standard configuration (single-output model)

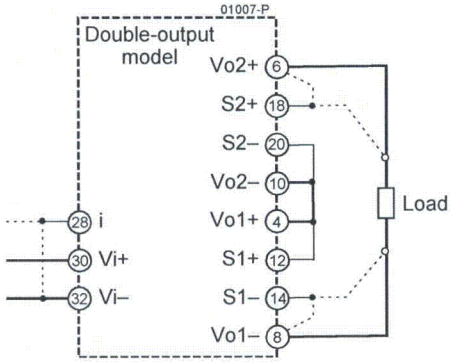


Fig. 2
Series output configuration of a double-output model. The second output is fully regulated.

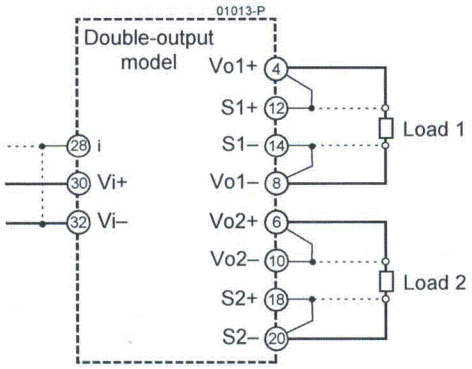


Fig. 3
Independent double-output configuration. Both outputs are fully regulated

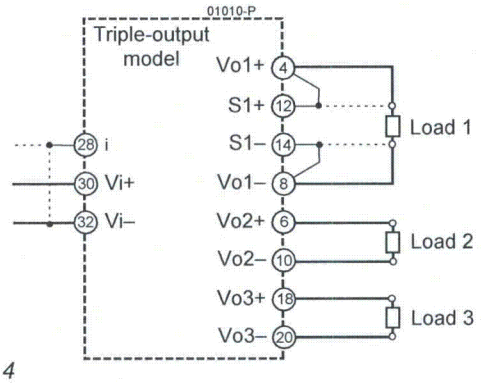


Fig. 4
Independent triple-output configuration. Output 3 is tracking

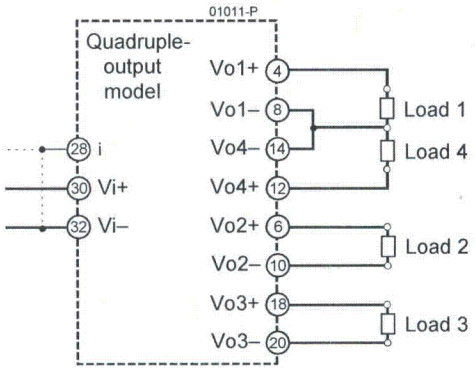


Fig. 5
Common ground configuration of output 1 with 4 and independent configuration of output 2 and 3

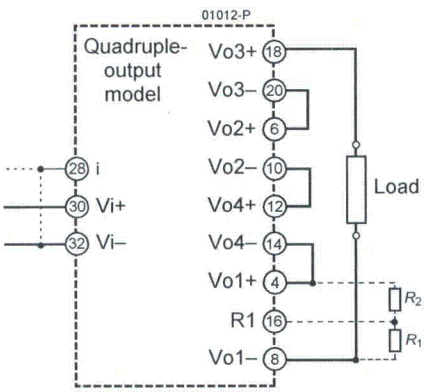


Fig. 6
Series configuration of all outputs (V_o = 96 V for xP4660). The R1-input influences only outputs 1 and 4. For the values of R1 and R2 see Output Voltage Adjust.

Functional Description

The power supplies are equipped with two independent flight-forward converters, switching 180° phase-shifted to minimize the ripple current at the input. They use primary and secondary control circuits in hybrid technology. The two converters, called "powertrains" (PT), each generate either a single output with synchronous rectifier or two isolated outputs, one fully regulated and the other one tracking (semi-regulated), thus providing up to four output voltages. In some models, both outputs of a powertrain are connected in parallel internally.

The highly efficient input filter together with very low input capacitance causes very low and short inrush current. After transformer isolation and rectification the output filter reduces ripple and noise to a minimum without affecting the dynamic response. Outputs 3 and 4, if available, are tracking (semi-regulated) and rely upon the close magnetic coupling of the transformer and the output inductor together with the circuit symmetry for their voltage regulation. A current limitation is located on the primary side of each powertrain limiting the total output current from that powertrain in overload conditions. This allows flex power operation of the outputs from each powertrain. All outputs can either be connected in series or in parallel; see *Electrical Output Data*.

An auxiliary converter provides the bias voltages for the primary and secondary referenced control logic and the option circuits. An oscillator generates a clock pulse of typically 307 kHz, which is fed to the control logic of each powertrain. The pulsewidth modulation and the magnetic feedback are provided by special ASICs. The converter is only enabled, if the input voltage is within the operating voltage range.

Double-output powertrains are equipped with a suppressor diode and an independant monitor sensing the output voltage of the tracking output. It shuts down the concerned powertrain, if an overvoltage occurs.

Single-output powertrains are protected by a suppressor diode.

The temperature of the heat sink is monitored and causes the converter to disable the outputs, until the temperature drops; then the converter will automatically resume.

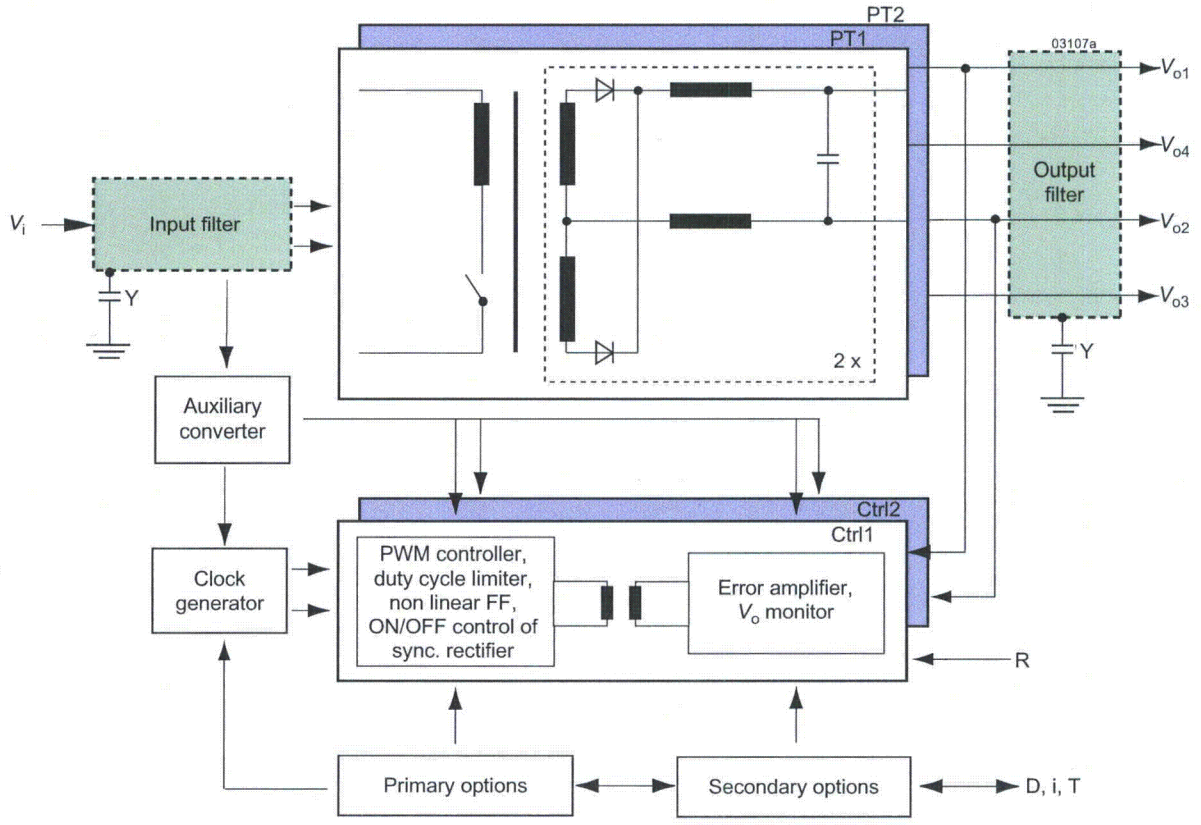


Fig. 7
Block diagram. Powertrains PT1 and PT2 have isolated outputs.
Pin allocation see table 12

Electrical Input Data

General Conditions:
– T_A = 25°C, unless T_C is specified
– Sense lines connected directly at the connector, inhibit (28) connected to Vi– (32)
– R input open

Table 2a: Input data

Input			BP			GP			CP			Unit
Characteristics		Conditions	min	typ	max	min	typ	max	min	typ	max	
V_i	Operating input voltage	I_o = 0 – $I_{o\,max}$ $T_{C\,min}$ – $T_{C\,max}$	16		36	21.6		50.4	33.6		75	V
$V_{i\,nom}$	Nominal input voltage			24			36			48		
Short term excursions	For ≤100 ms	without lockout	14.4		40				28.8			
	For ≤ 2 s											
	For ≤3 s	with lockout			50			63			100	
I_i	Typical input current [1]	$V_{i\,nom}$, $I_{o\,nom}$		5.6			3.7			2.8		A
$P_{i\,0}$	No-load input power [1]	$V_{i\,min}$ [1] – $V_{i\,max}$ I_o = 0	4		6.5	4		6.5	5		10	W
$P_{i\,inh}$	Idle input power [1 4]		1		1.5	1		1.5	1		1.5	
$I_{inr\,p}$	Peak inrush current [2]	$V_{i\,max}$, $I_{o\,max}$		61			64			66		A
$t_{inr\,rise}$	Rise time inrush			50			32			30		µs
t_r	Rise time inhibit [3]	$I_{o\,max}$ – $V_{i\,nom}$		5			5			5		ms
t_f	Fall time inhibit [3]			2			2			2		
$t_{d\,on}$	Start-up time [3]	0 → $V_{i\,min}$, $I_{o\,max}$		110						300		

Table 2b: Input data

Input			DP[2]			EP			Unit
Characteristics		Conditions	min	typ	max	min	typ	max	
V_i	Operating input voltage	I_o = 0 – $I_{o\,max}$ $T_{C\,min}$ – $T_{C\,max}$	40[2]		100.8	66		150	V
$V_{i\,nom}$	Nominal input voltage			72			110		
Short term excursions	For ≤ 100 ms	without lockout	36		115	57.6		184	
	For ≤ 2 s							168	
	For ≤3s	with lockout			134			200	
I_i	Typical input current [1]	$V_{i\,nom}$, $I_{o\,nom}$		1.9			1.2		A
$P_{i\,0}$	No-load input power [1]	$V_{i\,min}$ – $V_{i\,max}$ I_o = 0	5		11	5		12	W
$P_{i\,inh}$	Idle input power [1 4]		1		1.7	1.1		1.7	
$I_{inr\,p}$	Peak inrush current [2]	$V_{i\,max}$, $I_{o\,max}$		57			65		A
$t_{inr\,rise}$	Rise time inrush			20			20		µs
t_r	Rise time inhibit [3]	$I_{o\,max}$, $V_{i\,nom}$		5			5		ms
t_f	Fall time inhibit [3]			2			1		
$t_{d\,on}$	Start-up time [3]	0 → $V_{i\,min}$, $I_{o\,max}$					200		

[1] Typical values depending on model
[2] According to ETS 300132-2
[3] See fig. 16
[4] Converter inhibited

Input Fuse

A fuse mounted inside the converter protects against further damage in case of a failure. The fuse is not user-accessible. Reverse polarity at the input will cause the fuse to blow.

Table 3: Fuse specification

Model	Fuse type	Rating	Reference
BP	very fast blow	2× 10 A, 125 V	Littelfuse Pico 251
GP	very fast blow	2× 10 A, 125 V	Littelfuse Pico 251
CP	very fast blow	10 A, 125 V	Littelfuse Pico 251
DP	very fast blow	7 A, 125 V	Littelfuse Pico 251
EP	very fast blow	5 A, 250 V	Littelfuse Pico 263

Input Transient Protection

A VDR (Voltage Dependent Resistor), the input fuse, and a symmetrical input filter form an effective protection against input transients, which typically occur in most installations, but especially in battery-driven mobile applications.

Nominal battery voltages in use are: 24, 36, 48, 60, 72, 96, and 110 V. In most cases each nominal value is specified in a tolerance of –30% to +25%, with short excursions to ±40% or even more.

In some applications, surges according to RIA 12 are specified in addition to those defined in IEC 60571-1 or EN 50155. The power supply must not switch off during these surges, and since their energy can practically not be absorbed, an extremely wide input range is required. The P Series input range has been designed and tested to meet these requirements; see *Electromagnetic Immunity.*

Input Under- / Overvoltage Lockout

If the input voltage is below approx. 0.9 $V_{i\,min}$ or exceeds approx. 1.1 $V_{i\,max}$, an internally generated inhibit signal disables the output(s). However, short extentions specified in EN 50155 will be withstood without shutdown.

Inrush Current

The inherent inrush current value is lower than specified in the standard ETS 300132-2 (ver. 3.1). The units operate with relatively small input capacitance resulting in low inrush current of short duration. As a result in a power-bus system the units can be hot plugged-in or disconnected causing negligible disturbance at the input side.

Electrical Output Data

General Conditions:
– T_A = 25°C, unless T_C is specified.
– Sense lines connected directly at the connector, inhibit (28) connected to Vi– (32).
– R input not connected

Table 4a: Output data for single-output powertrains

Output	Single-output powertrain			3.3 V			5.1 V			12 V			Unit
Characteristics			Conditions	min	typ	max	min	typ	max	min	typ	max	
V_o	Output voltage [1]		$V_{i\,nom}$, $I_{o\,nom}$	3.28	3.3	3.32	5.07	5.1	5.13	11.94	12	12.06	V
V_{ow}	Worstcase output voltage		$V_{i\,min}$ – $V_{i\,max}$ $T_{C\,min}$ – $T_{C\,max}$ I_o = 0 – $I_{o\,max}$	3.24		3.35	5.02		5.18	11.82		12.18	
$V_{o\,P}$	Overvoltage protection [2]			6.45	6.8		6.45	6.8		14.3	15	15.8	
$I_{o\,nom}$	Nominal output current				15			12			5		A
$I_{o\,max}$	Max. output current		$V_{i\,min}$ – $V_{i\,max}$ $T_{C\,min}$ – $T_{C\,max}$		20			18			8		
I_{oL}	Output current limit [3]				22			19.8			8.8		
v_o	Output noise	Switch. frequ.	$V_{i\,nom}$, $I_{o\,max}$ BW = 20 MHz		5			5			15		mV_{pp}
		Total incl. spikes			20			20			30		
$v_{o\,d}$	Dynamic load regulation	Voltage deviation	$V_{i\,nom}$ $I_{o\,max} \leftrightarrow {}^1/_2\, I_{o\,max}$		0.7			0.8			1.2		V
t_d [5]		Recovery time			0.4			0.3			0.15		ms
$V_{o\,tr}$	Output voltage trim range (via R input)		1.1 $V_{i\,min}$ – $V_{i\,max}$ (0.1 – 1) $I_{o\,max}$ $T_{C\,min}$ – $T_{C\,max}$	1.79		3.63	2.75		5.61	6.5		13.2	V

[1] If the output voltages are increased above $V_{o\,nom}$ through R-input control or remote sensing, the output power should be reduced accordingly, so that $P_{o\,max}$ and $T_{C\,max}$ are not exceeded.
[2] Breakdown voltage of the incorporated suppressor diode at 10 mA (3.3 V, 5.1 V) or 1 mA (12 V). Exceeding this voltage might damage the suppressor diode.
[3] See *Output Current Limitation* and *Increased Output Power at Reduced Temperature*
[4] Measured according to IEC/EN 61204 with a probe described in annex A
[5] Recovery time until V_o returns to ±1% of V_o; see *Dynamic Load Regulation*.

Table 4b: Output data for single-output powertrains. General conditions as in table 4a

Output	Single-output powertrain		15 V			24 V			Unit
Characteristics		Conditions	min	typ	max	min	typ	max	
V_o	Output voltage [1]	$V_{i\,nom}$, $I_{o\,nom}$	14.93	15	15.08	23.88	24	24.12	V
V_{ow}	Worstcase output voltage	$V_{i\,min} - V_{i\,max}$ $T_{C\,min} - T_{C\,max}$ $I_o = 0 - I_{o\,max}$	14.78		15.23	23.64		24.36	
$V_{o\,P}$	Overvoltage protection [2]		17.1	18	18.9	28.5	30	31.5	
$I_{o\,nom}$	Nominal output current			4			2.5		A
$I_{o\,max}$	Max. output current	$V_{i\,min} - V_{i\,max}$ $T_{C\,min} - T_{C\,max}$		6.5			4		
I_{oL}	Output current limit [3]			7.2			4.4		
v_o	Output noise: Switch. frequ.	$V_{i\,nom}$, $I_{o\,max}$ BW = 20 MHz		15			15		mV_{pp}
	Output noise: Total incl. spikes			40			70		
$v_{o\,d}$	Dynamic load regulation: Voltage deviation	$V_{i\,nom}$ $I_{o\,max} \leftrightarrow {}^1/_2\, I_{o\,max}$		1.2			0.5		V
t_d [5]	Dynamic load regulation: Recovery time			0.2			0.15		ms
$V_{o\,tr}$	Output voltage trim range (via R input)	1.1 $V_{i\,min} - V_{i\,max}$ (0.1 – 1) $I_{o\,max}$ $T_{C\,min} - T_{C\,max}$	8.1		16.5	13		26.4	V

Table 4c: Output data for double-output powertrains. General conditions as in table 4a

Output	Double-output powertrain		12 V						Unit
			Main output			Tracking output			
Characteristics		Conditions	min	typ	max	min	typ	max	
V_o	Output voltage [1]	$V_{i\,nom}$, $I_{o\,nom}$	11.88	12	12.12	11.76	12	12.24	V
V_{ow}	Worstcase output voltage	$V_{i\,min} - V_{i\,max}$ $T_{C\,min} - T_{C\,max}$ $I_o = 0 - I_{o\,max}$	11.82		12.18	See *Output Voltage Regulation*			
$V_{o\,P}$	Overvoltage protection [2]			none		14.3	15	15.8	
$V_{o\,L}$	Overvoltage limitation [6]			none			14.4		
$I_{o\,nom}$	Nominal output current			2.5			2.5		A
$I_{o\,max}$	Max. output current	$V_{i\,min} - V_{i\,max}$ $T_{C\,min} - T_{C\,max}$		4			4		
I_{oL}	Output current limit [3]			4.4			4.4		
v_o	Output noise: Switch. frequ.	$V_{i\,nom}$, $I_{o\,max}$ BW = 20 MHz		15			15		mV_{pp}
	Output noise: Total incl. spikes			30			30		
$v_{o\,d}$	Dynamic load regulation: Voltage deviation	$V_{i\,nom}$ $I_{o\,max} \leftrightarrow {}^1/_2\, I_{o\,max}$		1.2			1.2		V
t_d [5]	Dynamic load regulation: Recovery time			0.15			0.15		ms
$V_{o\,tr}$	Output voltage trim range (via R input)	1.1 $V_{i\,min} - V_{i\,max}$ (0.1 – 1) $I_{o\,max}$ $T_{C\,min} - T_{C\,max}$	6.5		13.2	See *Output Voltage Regulation*			V

[1] If the output voltages are increased above $V_{o\,nom}$ through R-input control or remote sensing, the output power should be reduced accordingly, so that $P_{o\,max}$ and $T_{C\,max}$ are not exceeded.
[2] Breakdown voltage of the incorporated suppressor diode at 1 mA. Exceeding this voltage might damage the suppressor diode.
[3] See *Output Current Limitation* and *Increased Output Power at Reduced Temperature*
[4] Measured according to IEC/EN 61204 with a probe described in annex A
[5] Recovery time until V_o returns to ±1% of V_o; see *Dynamic Load Regulation*
[6] Output voltage limitation by an additional control loop

Table 4d: Output data for double-output powertrains. General conditions as in table 4a

Output	Double-output powertrain		15 V						24 V						Unit
			Main output			Tracking output			Main output			Tracking output			
Characteristics		Conditions	min	typ	max	min	typ	max	min	typ	max	min	typ	max	
V_o	Output voltage [1]	$V_{i\,nom}$, $I_{o\,nom}$	14.85	15	15.15	14.7	15	15.3	23.76	24	24.24	23.52	24	24.48	V
V_{ow}	Worstcase output voltage	$V_{i\,min} - V_{i\,max}$ $T_{C\,min} - T_{C\,max}$ $I_o = 0 - I_{o\,max}$	14.78		15.23	See *Output Voltage Regulation*			23.64		24.36	See *Output Voltage Regulation*			
$V_{o\,P}$	Overvoltage protection [2]		none			17.1	18	18.9	none			28.5	30	31.5	
$V_{o\,L}$	Overvoltage limitation [6]		none			17.6			none			28.8			
$I_{o\,nom}$	Nominal output current		2			2			1.25			1.25			A
$I_{o\,max}$	Max. output current	$V_{i\,min} - V_{i\,max}$ $T_{C\,min} - T_{C\,max}$	3.25			3.25			2			2			
I_{oL}	Output current limit [3]		3.6			3.6			2.2			2.2			
v_o	Output noise: Switch. frequ.	$V_{i\,nom}$, $I_{o\,max}$ BW = 20 MHz	15			15			15			15			mV_{pp}
	Output noise: Total incl. spikes		40			40			70			70			
$v_{o\,d}$	Dynamic load regulation: Voltage deviation	$V_{i\,nom}$ $I_{o\,max} \leftrightarrow {}^1/_2\, I_{o\,max}$	1.2			1.2			0.5			0.5			V
t_d [5]	Dynamic load regulation: Recovery time		0.2			0.2			0.15			0.15			ms
$V_{o\,tr}$	Output voltage trim range (via R input)	1.1 $V_{i\,min} - V_{i\,max}$ (0.1 – 1) $I_{o\,max}$ $T_{C\,min} - T_{C\,max}$	8.1		16.5	See *Output Voltage Regulation*			13		26.4	See *Output Voltage Regulation*			V

[1] If the output voltages are increased above $V_{o\,nom}$ through R-input control or remote sensing, the output power should be reduced accordingly, so that $P_{o\,max}$ and $T_{C\,max}$ are not exceeded.
[2] Breakdown voltage of the incorporated suppressor diode at 1 mA. Exceeding this voltage might damage the suppressor diode.
[3] See *Output Current Limitation* and *Increased Output Power at Reduced Temperature*
[4] Measured according to IEC/EN 61204 with a probe described in annex A
[5] Recovery time until V_o returns to ±1% of V_o; see *Dynamic Load Regulation*
[6] Output voltage limitation by an additional control loop

Parallel and Series Connection

The first outputs of power trains with equal nominal output voltage can be connected in parallel. Where available, we recommend ordering of option T.

Any output can be connected in series with any other output. If the main and the tracking output of the same power train are connected in series, consider that the effect of the R-input is doubled.

Notes:

If tracking outputs are not used, connect them in parallel to the respective regulated main output.

Connection of several outputs in parallel should include measures to approximate all output currents. 3.3 and 5 V outputs with option T have current share pins (T or T1), which must be interconnected. For other outputs, the load lines should exhibit similar resistance. Parallel connection of regulated outputs without such precautions is not recommended.

The maximum output current of a serial-connected outputs is limited by the output with the lowest current limit.

Rated output voltages above 48 V (SELV = Safety Extra Low Voltage) require additional safety measures in order to comply with international safety requirements.

Parallel operation of two double-output converters with series-connected outputs is shown in fig. 9. The link

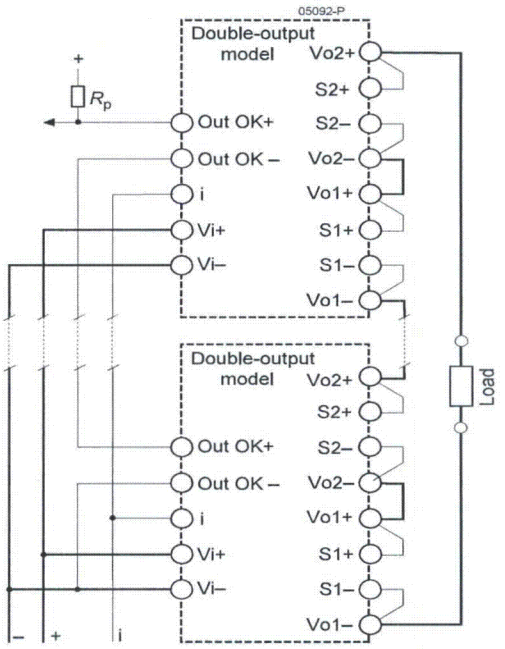


Fig. 8
Series connection of double-output models. Sense lines connected at the connector.

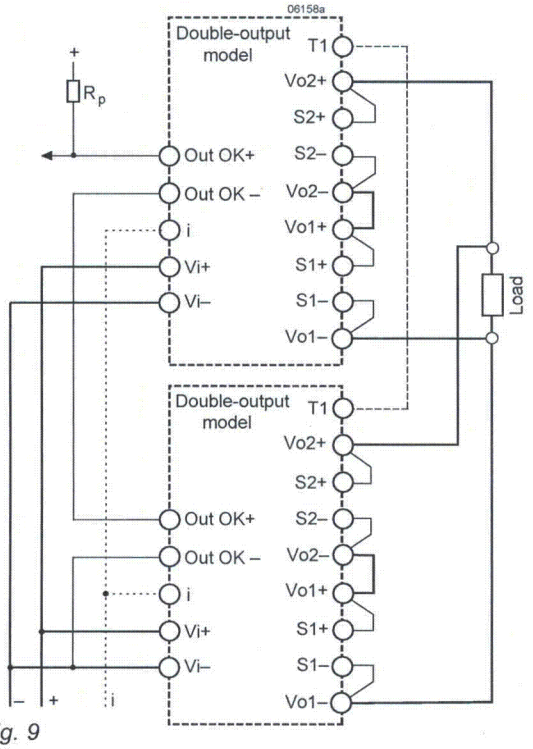


Fig. 9
Parallel operation of 2 double-output converters with series-connected outputs.

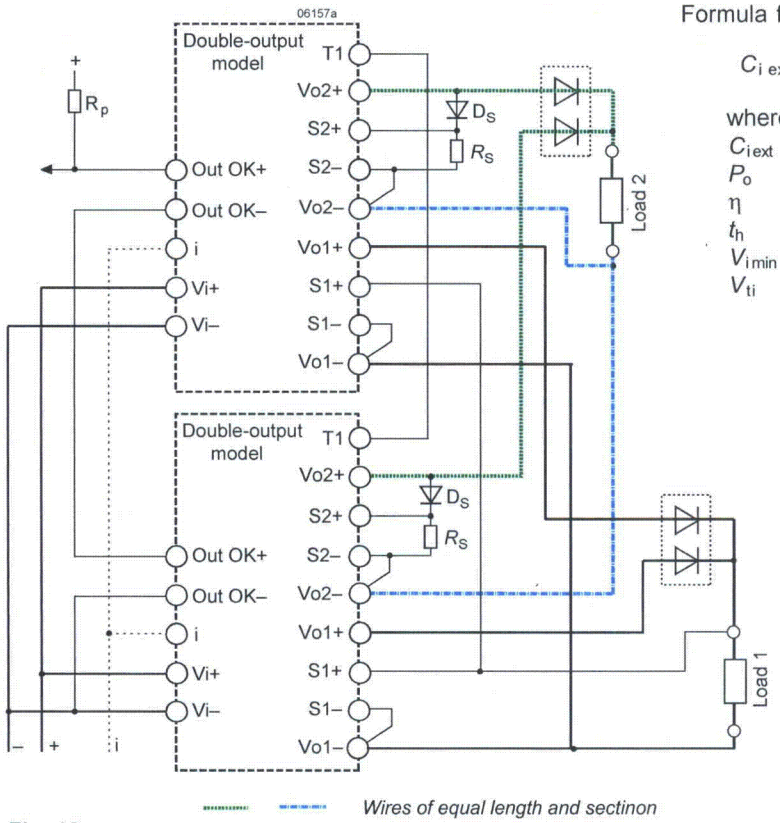


Fig. 10
Redundant configuration

between the T1 pins ensures proper current sharing, even though only the first outputs are influenced. Sense lines are connected directly at the connector, and load lines have equal length and section.

Redundant Systems

An example of a redundant system using converters with 2 regulated ouputs (xP2020) is shown in fig. 10. Load 1 is powered with 5.1 V and load 2 with 12 V.

The converters are separated with ORing diodes. If one converter fails, the remaining one still delivers the power to the loads. If more power is needed, the system may be extended to more parallel converters (n+1 redundancy).

Current sharing of the 5.1 V outputs is ensured by interconnected T1 pins, whereas the sense lines are connected after the ORing diodes to maintain the correct output voltage.

For the 12 V outputs, no current feature is available. As a result, 2 little diodes D_s (loaded by little resistors R_s) simulate the voltage drop of the ORing diodes. Reasonable current sharing is provided by load lines of equal length and section.

Hold-up Time

The converters provide virtually no hold-up time. If a hold-up time is required, use external output capacitors or decoupling diodes and input capacitors of adequate size.

Formula for additional external input capacitor:

$$C_{i\,ext} = \frac{2 \cdot P_o \cdot t_h \cdot 100}{(V_{ti}^2 - V_{i\,min}^2) \cdot \eta}$$

whereas:

$C_{i\,ext}$ = external input capacitance [mF]
P_o = output power [W]
η = efficiency [%]
t_h = hold-up time [ms]
$V_{i\,min}$ = minimum input voltage [V]
V_{ti} = threshold level [V]

Output Voltage Regulation

Line and load regulation of the regulated outputs is so good that input voltage and output current have virtually no influence to the output voltage.

However, if the tracking output is not loaded, the second control loop may slightly reduce the voltage of the main output. Thus, unused tracking outputs should be connected in parallel to the respective main output.

The dynamic load regulation is shown in fig. 11.

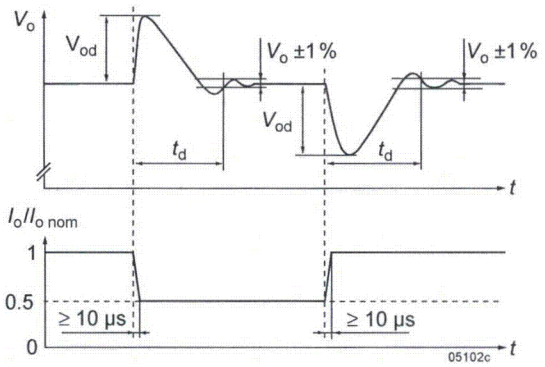


Fig. 11
Typical dynamic load regulation of output voltage

Tracking Outputs

The main outputs 1 and 2 are regulated to $V_{o\,nom}$ independent of the output current. If the loads on outputs 3 and 4 are too low (<10% of $I_{o\,nom}$), their output voltage tends to rise. V_{o3} and V_{o4} depend upon the load distribution: If all outputs are loaded with at least 10% of $I_{o\,nom}$, V_{o3} and V_{o4} remain within ±5% of $V_{o\,nom}$. The following diagrams show the regulation of the tracking outputs under different load conditions up to the current limit. If $I_{o1} = I_{o4}$ and $I_{o2} = I_{o3}$ or if the tracking outputs are connected in series with their respective regulated outputs, then V_{o3} and V_{o4} remain within ±1% of $V_{o\,nom}$ provided that the load is at least $I_{o\,min}$. A 2nd control loop protects the tracking outputs against overvoltage by reducing the voltage of the respective regulated main output.

Because the P Series uses main transformers and main chokes in planar technology, the tracking outputs follow the main outputs very closely.

Note: If the tracking output (V_{o3} or V_{o4} is not loaded, it should be connected in parallel to the respective main output (V_{o3} parallel to V_{o2}, V_{o4} parallel to V_{o1}).

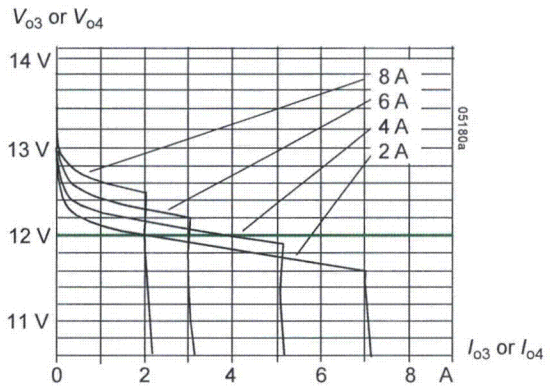


Fig. 12
12 V tracking output V_{o4} versus I_{o4} (powertrain 1) or V_{o3} versus I_{o3} (powertrain 2). $V_i = V_{i\,nom}$

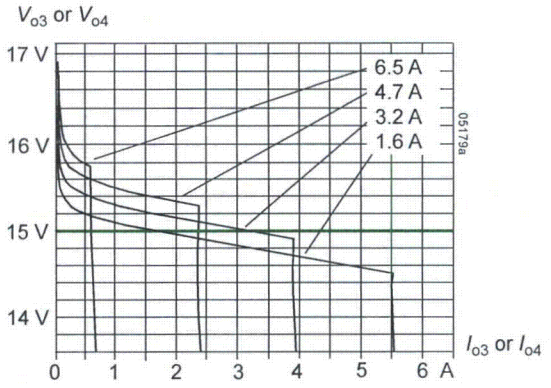


Fig. 13
15 V tracking output $V_o = f(I_o)$, $V_i = V_{i\,nom}$

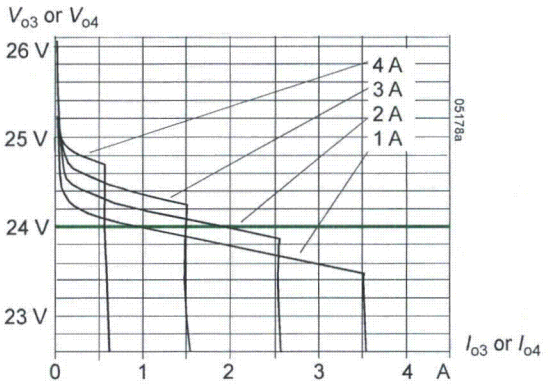


Fig. 14
24 V tracking output $V_o = f(I_o)$, $V_i = V_{i\,nom}$

Hot Swap

Important: For applications using the hot swap capabilities, dynamic output voltage changes during plug-in and plug-out operations should be considered.

Output Current Limitation

All outputs are continously protected against open-circuit (no load) and short-circuit by an electronic current limitation.

Single- and double-output powertrains have a rectangular current limitation characteristic. In double output power-trains only the total current is limited allowing free choice of load distribution between the two outputs of each power train up to a total $I_{o1} + I_{o4} = I_{o\,max}$ or $I_{o2} + I_{o3} = I_{o\,max}$.

Thermal Considerations

If a converter is mounted upright in free air, allowing unrestricted convection cooling, and is operated at its nominal input voltage and output power at $T_{A\ max}$ (see table *Temperature specifications*), the temperature measured at the measurement point on the case T_C (see *Mechanical Data)* will approach $T_{C\ max}$ after an initial warm-up phase. However the relationship between T_A and T_C depends heavily on the operating conditions and system integration. The thermal conditions are influenced significantly by the input voltage, the output current, airflow, and the temperature of the adjacent elements and surfaces. $T_{A\ max}$ is therefore contrary to $T_{C\ max}$ only an indicative value.

Thermal Protection

A temperature sensor fitted on the main PCB disables the output, when the case temperature exceeds $T_{C\ max}$. The converter automatically resumes, when the temperature drops below this limit. A temperature sensor on each power train reduces the output current limit of that power train, when the temperature exceeds a safe level.

Output Power at Reduced Temperature

Operating the converters with an output current between $I_{o\ nom}$ and $I_{o\ max}$ requires a reduction in maximum ambient temperature or forced air cooling in order to keep T_C below 95 °C. When $T_{C\ max}$ is exceeded, the thermal protection is activated and disables the outputs.

Note: Forced cooling or an additional heat sink can improve the reliability or allow T_A to go beyond $T_{A\ max}$, provided that $T_{C\ max}$ is not exceeded. In rack systems without proper thermal management the converters should not be packed too closely together! In such cases the use of a 5 or 6TE front panel is recommended.

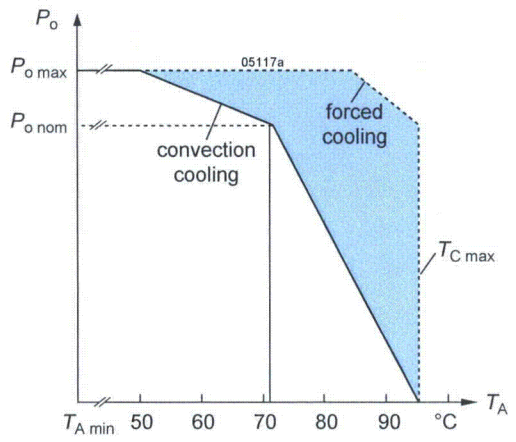


Fig. 15
Output power derating versus T_A.

Auxiliary Functions

Primary Inhibit (Remote On / Off)

The inhibit input enables (logic low, pull down) or disables (logic high, pull up or open-circuit) the output, if a logic signal (TTL, CMOS) is applied. In systems consisting of several converters, this feature may be used to control the activation sequence by logic signals or to enable the power source to start up, before full load is applied.

Note: If this function is not used, pin 28 must be connected with pin 32, otherwise the internal logic will disable the output.

Table 5: Inhibit characteristics

Characteristic			Conditions	min	typ	max	Unit
V_{inh}	Inhibit Voltage	V_o = on	$V_{i\,min}$ - $V_{i\,max}$	−50		0.8	V
		V_o = off	$T_{C\,min}$ - $T_{C\,max}$	2.4		50	
I_{inh}	Inhibit current		V_{inh} = −50 V V_{inh} = 0 V V_{inh} = 50 V		−1000 −40 900		µA

Note: The secondary referenced inhibit function, refers to the description of option i.

The output response after enabling or disabling the output by the inhibit input is shown in the figure below. See also *Input Data*.

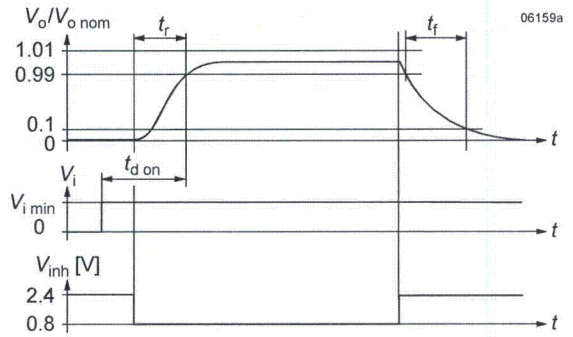


Fig. 16
Output response as a function of V_i (on/off switching) or inhibit control

Output Voltage Adjust of V_{o1} and V_{o4}

Note: With open R input, $V_o = V_{o\,nom}$.

The converters offer adjust of the voltage of powertrain 1. Powertrain 2 can not be adjusted. The programming is performed either by an external control voltage V_{ext} or an external resistor R_1 or R_2, connected to the R-input. Trimming is limited to the values given in the table *Electrical Output Data*.

Note: With open R input, $V_o = V_{o\,nom}$.

With double output powertrains, both outputs are influenced by the R-input setting simultaneously.

Caution: To prevent damage, V_{ext} should not exceed 20 V, nor be negative.

Note: If output voltages are set higher than $V_{o\,nom}$, the output currents should be reduced accordingly, so that the maximum specified output power is not exceeded.

a) Adjustment by means of an external voltage:

$$V_{ext} \approx \frac{2.72\ V_{o1}}{V_{o\,nom}} - 0.28\ V$$

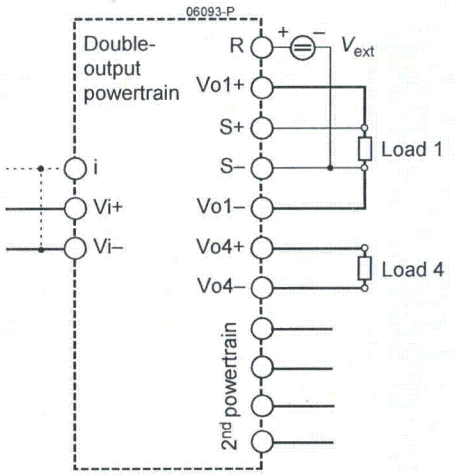


Fig. 17
Output adjust of V_{o1} and V_{o4} with an external voltage V_{ext}. The other outputs are not influenced.

b) Adjustment by means of an external resistor:

The resistor can either be connected between the pins R (16) and S− (14) to set $V_o < V_{o\,nom}$, or between the pins R (16) and S+ (12) to set $V_o > V_{o\,nom}$.

Note: R inputs of n converters with paralleled outputs may be connected together, but if only one external resistor is used, its value should be R_1/n or R_2/n.

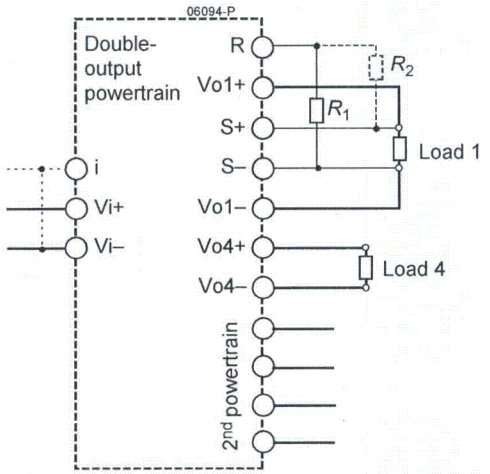


Fig. 18
Output adjust of V_{o1} and V_{o4} using R_1 or R_2. The other outputs are not influenced.

Table 6a: R_1 for $V_o < V_{o\,nom}$; approximate values ($V_{i\,nom}$, $I_{o\,nom}$, series E 96 resistors); R_2 not fitted

$V_{o\,nom}$ = 3.3 V		$V_{o\,nom}$ = 5.1 V		$V_{o\,nom}$ = 12 V			$V_{o\,nom}$ = 15 V			$V_{o\,nom}$ = 24 V		
V_o (V)	R_1 [kΩ]	V_o (V)	R_1 [kΩ]	V_o [V] [1]		R_1 [kΩ]	V_o [V] [1]		R_1 [kΩ]	V_o [V] [1]		R_1 [kΩ]
2.0	5.62	4.0	14.0	6.5	13.0	4.22	8.0	16.0	4.12	14.0	28.0	5.23
2.1	6.49	4.1	15.8	7.0	14.0	5.11	8.5	17.0	4.75	15.0	30.0	6.19
2.2	7.50	4.2	18.2	7.5	15.0	6.19	9.0	18.0	5.49	16.0	32.0	7.5
2.3	8.66	4.3	21.0	8.0	16.0	7.5	9.5	19.0	6.34	17.0	34.0	9.31
2.4	10.2	4.4	24.3	8.5	17.0	9.09	10.0	20.0	7.5	18.0	36.0	11.5
2.5	12.1	4.5	29.4	9.0	18.0	11.5	10.5	21.0	8.87	19.0	38.0	14.7
2.6	14.3	4.6	36.5	9.5	19.0	14.7	11.0	22.0	10.5	20.0	40.0	19.6
2.7	17.4	4.7	47.5	10.0	20.0	19.6	11.5	23.0	12.7	20.5	41.0	22.6
2.8	22.1	4.8	63.4	10.5	11.0	27.4	12.0	24.0	15.4	21.0	42.0	27.4
2.9	28.7	4.9	97.6	11.0	22.0	43.2	12.5	25.0	29.6	21.5	43.0	34.0
3.0	39.2	5.0	200.0	11.5	23.0	88.7	13.0	26.0	25.5	22.0	44.0	43.2
3.1	61.9						13.5	27.0	34.8	22.5	45.0	59.0
3.2	12.7						14.0	28.0	54.9	23.0	46.0	88.7
							14.5	29.0	110.0	23.5	47.0	182.0

Table 6b: R_2 for $V_o > V_{o\,nom}$; approximate values ($V_{i\,nom}$, $I_{o\,nom}$, series E 96 resistors); R_1 not fitted

$V_{o\,nom}$ = 3.3 V		$V_{o\,nom}$ = 5.1 V		$V_{o\,nom}$ = 12 V			$V_{o\,nom}$ = 15 V			$V_{o\,nom}$ = 24 V		
V_o (V)	R_1 [kΩ]	V_o (V)	R_1 [kΩ]	V_o [V] [1]		R_1 [kΩ]	V_o [V] [1]		R_1 [kΩ]	V_o [V] [1]		R_1 [kΩ]
3.4	47.5	5.2	226.0	12.2	24.4	1100.0	15.3	30.6	1130.0	24.5	49.0	1820.0
3.5	24.3	5.3	115.0	12.4	24.8	499.0	15.5	31.0	665.0	25.0	50.0	909.0
3.6	16.3	5.4	78.7	12.6	25.2	332.0	15.7	31.4	475.0	25.5	51.0	604.0
		5.5	59.0	12.8	25.6	255.0	16.0	32.0	332.0	26.0	52.0	464.0
		5.6	48.7	13.0	26.0	205.0	16.2	32.4	280.0	26.4	52.8	392
				13.2	26.4	174.0	16.5	33.0	232.0			

[1] First column: single output powertrains or double output powertrains with separated/paralleled outputs, second column: outputs in series connection.

Sense Lines

Important: Sense lines should always be connected. Incorrectly connected sense lines may damage the converter. If sense lines are left open-circuit, the output voltages will be inaccurate.

This feature enables compensation of voltage drop across the connector contacts and the load lines including ORing diodes in true redundant systems.

Applying generously dimensioned cross-section load leads avoids troublesome voltage drop. To minimize noise pick-up, wire sense lines parallel or twisted to the respective output line. To be sure, connect the sense lines directly at the female connector.

The voltage difference between any sense line and its respective power output pin (as measured on the connector) should not exceed the following values at nominal output voltage.

Table 7: Voltage compensation allowed using sense lines

Output type	Total drop	Negative line drop
3.3, 5.1 V output	<0.5 V	<0.25 V
12, 15, 24 V output	<1.0 V	<0.5 V

Electromagnetic Compatibility (EMC)

A metal oxide resistor (VDR) together with an input fuse and filter form an effective protection against high input transient voltages, which typically occur in most installations, but especially in battery-driven mobile applications. The P series has been successfully tested to the following specifications:

Electromagnetic Immunity

Table 8: Immunity type tests

Phenomenon	Standard	Level	Coupling mode[1]	Value applied	Waveform	Source imped.	Test procedure	In oper.	Perf. crit.[2]
Supply related surge	RIA 12	B	+i/–i	1.5 • V_{batt}	0.1/1/0.1 s	0.2 Ω	1 positive surge	yes	A
	EN 50155			1.4 • V_{batt}		1 Ω			
Direct transients	RIA 12 EN 50155: 1995	D[4]	–i/c, +i/–i	1800 V_p	5/50 µs	5 Ω	5 pos. and 5 neg. impulses	yes	B
		G[5]		8400 V_p	0.05/0.1 µs	100 Ω			
Indirect coupled transients		H	–o/c, +o/–o, –o/–i	1800 V_p	5/50 µs				
		L		8400 V_p	0.05/0.1 µs				
Electrostatic discharge (to case)	IEC/EN 61000-4-2	4[6]	contact discharge	8000 V_p	1/50 ns	330 Ω	10 positive and 10 negative discharges	yes	B
			air discharge	15000 V_p					
Electromagnetic field, mobile phone	IEC/EN 61000-4-3	x[7]	antenna	20 V/m	AM 80% 1 kHz	n.a.	80 – 1000 MHz	yes	A
	ENV 50204	x[10]	antenna	20 V/m	50% duty cycle 200 kHz repetition		900 ±5 MHz	yes	A
Electrical fast transients/burst	IEC/EN 61000-4-4	4[8]	capacitive, o/c	2000 V_p	bursts of 5/50 ns 5 kHz over 15 ms; burst period: 300 ms	50 Ω	60 s positive 60 s negative transients per coupling mode	yes	B
			direct,+i/c, –i/c, +i/–i	4000 V_p					
Surges	IEC/EN 61000-4-5	3[3]	+i/c, –i/c	2000 V_p	1.2/50 µs	12 Ω	5 pos. and 5 neg. surges per coupling mode	yes	B
		2[3]	+i/–i	1000 V_p		2 Ω			
Conducted disturbances	IEC/EN 61000-4-6	3[9]	i, o, signal wires	10 VAC (140 dBµV)	AM 80% 1 kHz	150 Ω	0.15 – 80 MHz	yes	A

[1] i = input, o = output, c = case.
[2] A = Normal operation, no deviation from specs, B = Temporary deviation from specs possible.
[3] Measured with an external input capacitor (to prevent oscillations)
[4] Corresponds to EN 50155:2001, waveform A, and EN 50121-3-2:2000, table 7.2.
[5] Corresponds to EN 50155:2001, waveform B.
[6] Corresponds to EN 50121-3-2:2000, table 9.2.
[7] Corresponds to EN 50121-3-2:2000, table 9.1, and EN 50121-5-2:2000, table 1.1.
[8] Corresponds to EN 50121-3-2:2000, table 7.1.
[9] Corresponds to EN 50121-3-2:2000, table 7.4.
[10] Fulfills also EN 50121-5:2000, table 1.2, where ENV 50204 is referenced.

Electromagnetic Emissions

Table 9: Emissions at $V_{i\,nom}$ and $I_{o\,nom}$

Types	Level according to EN 55011 / EN 55022	
	≤30 MHz	>30 MHz
BP 2320 CP 1001	B B	
EP 3020 EP 4660	B B	

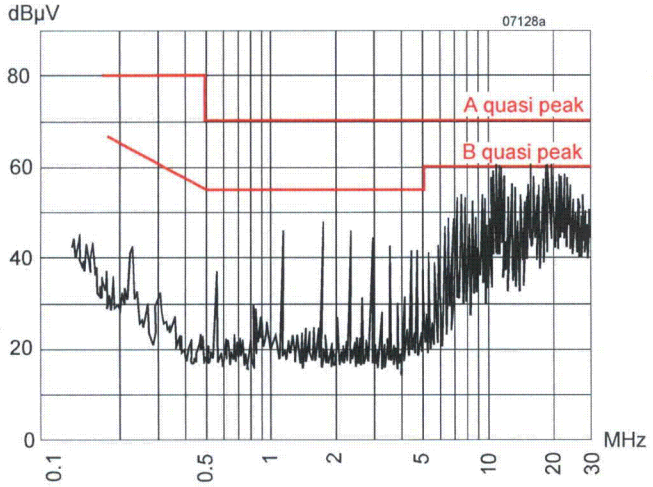


Fig. 19
BP 2320-7RD
Typical disturbance voltage at the input ($V_{i\,nom}$, $I_{i\,nom}$, resitive load, quasi peak).

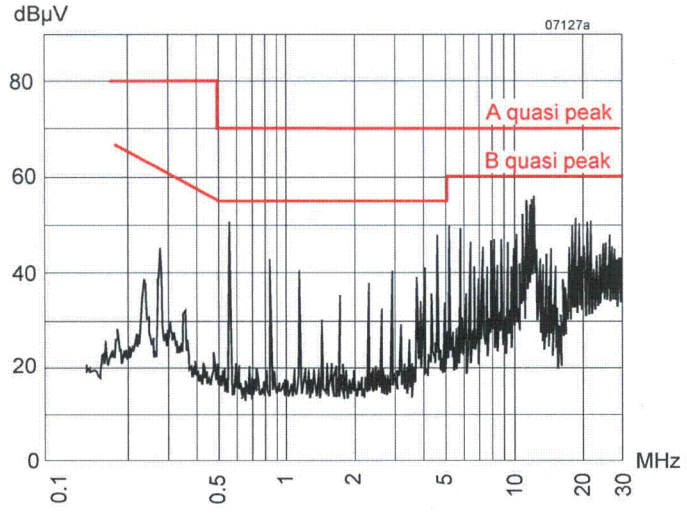


Fig. 20
CP 1001-7RB1
Typical disturbance voltage at the input ($V_{i\,nom}$, $I_{i\,nom}$, resitive load, quasi peak).

Immunity to Environmental Conditions

Table 10: Mechanical and climatic stress

Test method		Standard	Test conditions		Status
Cab	Damp heat steady state	IEC/EN 60068-2-78 MIL-STD-810D section 507.2	Temperature: Relative humidity: Duration:	40 $^{\pm 2}$ °C 93 $^{+2/-3}$ % 56 days	Converter not operating
Kb	Salt mist, cyclic (sodium chloride NaCl solution)	IEC/EN 60068-2-52	Concentration: Storage: Number of cycles	5% (30°C) for 2 h 40°C, 93% rel. humidity for 22 h 3 (= 3 days)	Converter not operating
Eb	Bump (half-sinusoidal)	IEC/EN 60068-2-29 MIL-STD-810D section 516.3	Acceleration amplitude: Bump duration: Number of bumps:	25 g_n = 245 m/s^2 11 ms 6000 (1000 in each direction)	Converter operating
Fc	Vibration (sinusoidal)	IEC/EN 60068-2-6 MIL-STD-810D section 514.3	Acceleration amplitude: Frequency (1 Oct/min): Test duration:	0.35 mm (10 – 60 Hz) 5 g_n = 49 m/s^2 (60 - 2000 Hz) 10 – 2000 Hz 7.5 h (2.5 h in each axis)	Converter operating
Ea	Shock (half-sinusoidal)	IEC/EN 60068-2-27 MIL-STD-810D section 516.3	Acceleration amplitude: Bump duration: Number of bumps:	50 g_n = 490 m/s^2 11 ms 18 (3 in each direction)	Converter operating
--	Shock	EN 50155 / EN 61373 sect. 10, class A and B body mounted [1]	Acceleration amplitude: Bump duration: Number of bumps:	5.1 g_n 30 ms 18 (3 in each direction)	Converter operating
Fda	Random vibration wide band Reproducibility high	IEC/EN 60068-2-35 DIN 40046 part 23	Acceleration spectral density: Frequency band: Acceleration magnitude: Test duration:	0.05 g_n^{2}/Hz 20 – 500 Hz 4.9 $g_{n\ rms}$ 3 h (1 h in each axis)	Converter operating
--	Simulated long life testing at increased random vibration levels	EN 50155 / EN 61373 sect. 9, cat 1, class B, body mounted [1]	Acceleration spectral density: Frequency band: Acceleration magnitude: Test duration:	0.02 g_n^{2}/Hz 5 – 150 Hz 0.8 $g_{n\ rms}$ 15 h (5 h in each axis)	Converter operating

[1] Body mounted = chassis of a railway coach

Temperatures

Table 11: Temperature specifications, valid for an air pressure of 800 – 1200 hPa (800 – 1200 mbar)

Temperature			-7 (option)			-9 (standard)			Unit
Characteristics		Conditions	min	typ	max	min	typ	max	
T_A	Ambient temperature	Converter operating [1]	–25		71	–40		71	°C
T_C	Case temperature [2]		–25		95 [1]	–40		95 [1]	
T_S	Storage temperature	Non operational	–40		100	–55		100	
$R_{th\ C\text{-}A}$	Thermal resistance case to ambient in still air			2			2		K/W

[1] Operation with $P_{o\ max}$ requires reduction to $T_{A\ max}$ = 50 °C, $T_{C\ max}$ = 85° C respectively; see *Thermal Considerations*.
[2] Overtemperature shut-down at T_C >95 °C (PTC)

Reliability

Table 12: MTBF and device hours

Ratings at specified Case Temperature	Model	Ground benign 40 °C	Ground fixed 40 °C	Ground fixed 70 °C	Ground mobile 50 °C	Device hours [1]
MTBF acc. to MIL-HDBK-217F, notice 2	CP 3000	340 000 h	88 000 h	42 000 h	40 000 h	7 670 000

[1] Statistical values, based on an average of 4300 working hours per year and in general field use over 5 years; upgrades, customer-induced errors excluded.

Mechanical Data

The converters are designed to be inserted in a 19" rack acording to IEC 60297-3. Dimensions in mm.

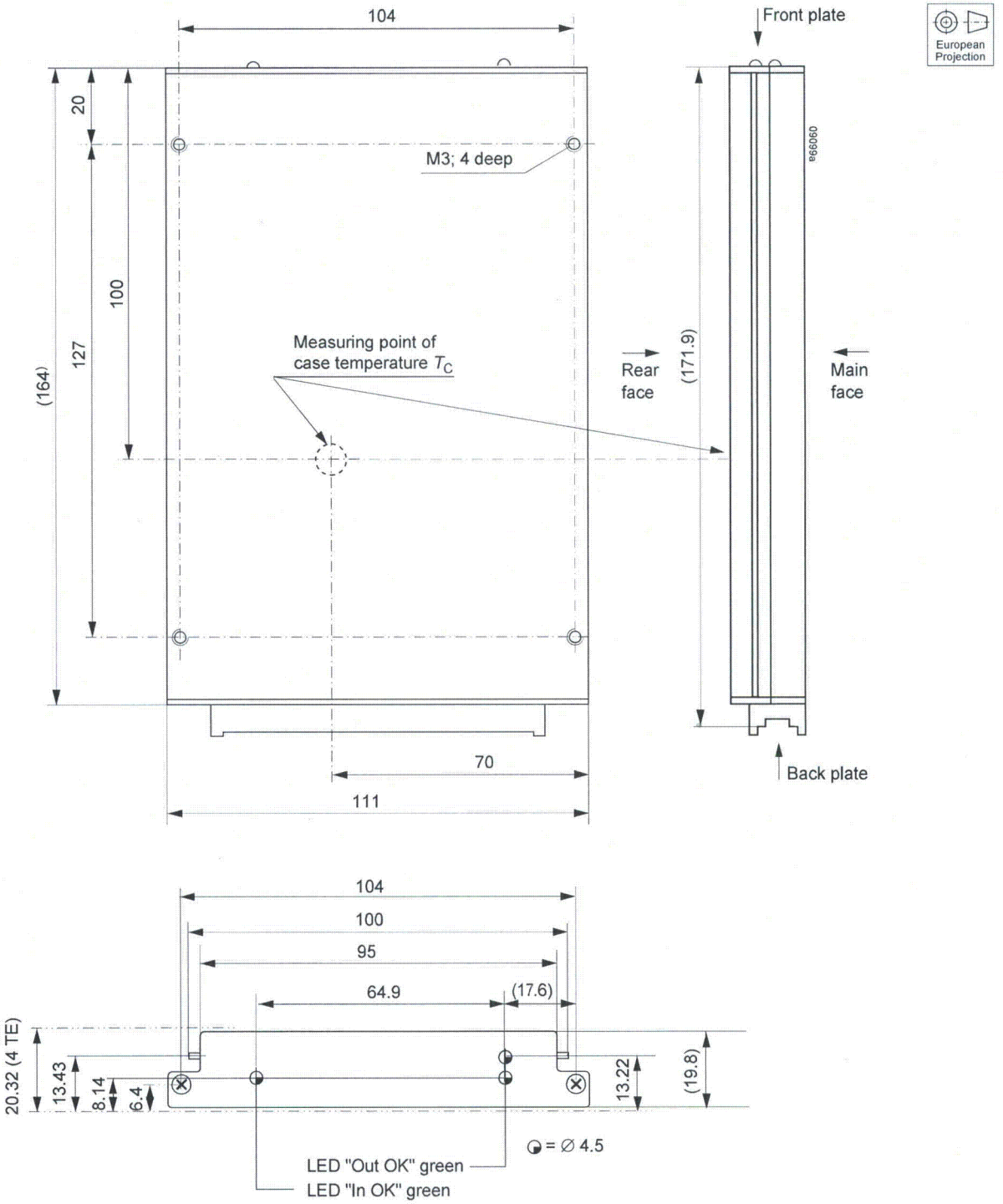


Fig. 21
Case Q04, weight app. 500 g
Aluminium, fully enclosed,
black finish and self cooling

Note: Long case, elongated by 60 mm for 220 mm rack depth is available on request.

Safety and Installation Instructions

Connector Pin Allocation

The connector pin allocation table defines the electrical potentials and the physical pin positions on the H15 and H15S2 connector. Pin no. 26, protective earth, is a leading pin to ensure that it makes contact with the female connector first.

Notes: The current through each standard H15 contact depends on the female connector, the ambient temperature, and the air flow in the region of the connector. We recommend to limit the mean current to 15 A at 50 °C and to 13 A at 71 °C.

High currents require a large cross-sectional area of the connections to the female contacts. We recommend solder or screw terminal contacts. Each faston connection exhibits a resistance of max. 8 mΩ, which makes it less suitable for high currents.

For single-output models with option K, always both output contacts must be used and connected in parallel to the load with large cross-sectional area wires or thick copper lands.

High-current contacts of P1000 models exhibit no restriction of the output current. Their resistance is only 1 mΩ.

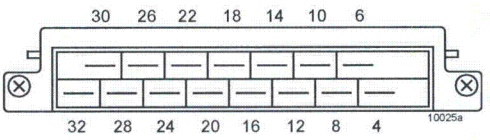


Fig. 22
View of male standard H15 connector

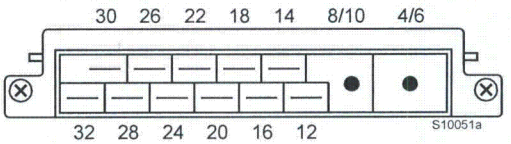


Fig. 23
View of male H15S2 connector (with high-current contacts) used in P1000 and P1100 without option K

Table 13: Pin allocation

Pin	P 1000		P2000		P3000		P4000	
4[1]	Vo+	Output 1 pos.	Vo1+	Output 1 pos.	Vo1+	Output 1 pos.	Vo1+	Output 1 pos.
6[1]	Vo+	Output 1 pos.	Vo2+	Output 2 pos.	Vo2+	Output 2 pos.	Vo2+	Output 2 pos.
8[2]	Vo–	Output 1 neg.	Vo1–	Output 1 neg.	Vo1–	Output 1 neg.	Vo1–	Output 1 neg.[6]
10[2]	Vo–	Output 1 neg.	Vo2–	Output 2 neg.	Vo2–	Output 2 neg.	Vo2–	Output 2 neg.
12	S+	Sense +	S1+	Sense 1 +	S1+	Sense 1 +	Vo4+	Output 4 pos.
14	S–	Sense –	S1–	Sense 1 –	S1–	Sense 1 –	Vo4–	Output 4 neg.[6]
16	R	Adjust of V_o	R1	Adjust of V_{o1}	R1	Adjust of V_{o1}	R1	Adjust of $V_{o1/4}$
			T1	Current share[3]	T1	Current share[3]		
18	T[7]	Current share	S2+	Sense 2 +	Vo3+	Output 3 pos.	Vo3+	Output 3 pos.
20	n.c.	Not connected	S2–	Sense 2 –	Vo3–	Output 3 neg.	Vo3–	Output 3 neg.
22	n.c.	Not connected	n.c.	Not connected	n.c.	Not connected	n.c.	Not connected
	Out OK+	Out OK+[4]	Out OK+	Out OK+[4]	Out OK+	Out OK+[4]	Out OK+	Out OK+[4]
	i+	Inhibit second.[5]	i+	Inhibit second.[5]	i+	Inhibit second.[5]	i+	Inhibit second.[5]
24	n. c.	Not connected	n.c.	Not connected	n.c.	Not connected	n.c.	Not connected
	Out OK–	Out OK–[4]	Out OK–	Out OK–[4]	Out OK–	Out OK–[4]	Out OK–	Out OK–[4]
	i–	Inhibit second.[5]	i–	Inhibit second.[5]	i–	Inhibit second.[5]	i–	Inhibit second.[5]
26	⏚	Prot. earth PE	⏚	Prot. earth PE	⏚	Prot. earth PE	⏚	Prot. earth PE
28	i	Inhibit primary	i	Inhibit primary	i	Inhibit primary	i	Inhibit primary
30	Vi+	Input pos.	Vi+	Input pos.	Vi+	Input pos.	Vi+	Input pos.
32	Vi–	Input neg.	Vi–	Input neg.	Vi–	Input neg.	Vi–	Input neg.

[1] Pin 4/6 (high-current contact) for P1000 models with 3.3 V or 5.1 V output (H15S2 connector)
[2] Pin 8/10 (high-current contact) for P1000 models with 3.3 V or 5.1 V output (H15S2 connector)
[3] Option T1 for 3.3 V and 5.1 V powertrains: Only I_{o1} is influenced
[4] Option D
[5] Option i
[6] Powertrains with 5.1 V and 3.3 V outputs have a common return: Vo1– and Vo4– are connected together.
[7] Not connected, if option T is not fitted.

Installation Instructions

These converters are components, intended exclusively for inclusion within other equipment by an industrial assembly process or by a professionally competent person. Installation must strictly follow the national safety regulations in respect of the enclosure, mounting, creepage distances, clearance, casualty, markings and segregation requirements of the end-use application.

Connection to the system shall be made via the female connector H15 or H15S2 (see *Accessories*). Other installation methods may not meet the safety requirements. Check for hazardous voltages before altering any connections. Pin 26 (PE) is a leading pin and is reliably connected to the case. For safety reasons it is essential to connect this pin to the protective earth of the supply system.

The Vi– input (pin 32) is internally fused. This fuse is designed to protect the converter against overcurrent caused by a failure, but may not be able to satisfy all requirements. External fuses in the wiring to one or both input pins (no. 30 and/or no. 32) may therefore be necessary to ensure compliance with local requirements.

Important: Whenever the inhibit function is not in use, pin 28 (i) should be connected to pin 32 (Vi–) to enable the output(s).

Do not open the converters, or the warranty will be invalidated. Make sure that there is sufficient airflow available for convection cooling. This should be verified by measuring the case temperature at the specified measuring point, when the converter is operated in the end-use application. $T_{C\,max}$ should not be exceeded. Ensure that a failure of the converter does not result in a hazardous condition; see also *Safety of Operator-Accessible Output Circuits*.

Standards and Approvals

The P Series converters are approved according to the safety standards IEC 60950-1, EN 60950-1, UL 60950-1, and CSA 60950-1.

They have been evaluated for:

- Class I equipment
- Building in
- Double or reinforced insulation based on 250 VAC or 240 VDC between input and output and between input and auxiliary circuits
- Overvoltage category II
- Functional insulation between output(s) and case
- Functional insulation between the outputs
- Pollution degree 2 environment
- The converters fulfill the requirements of a fire enclosure.

CB-scheme is available (CB 06 07 24238 800).

The converters are subject to manufacturing surveillance in accordance with the above mentioned UL standards and with ISO 9001:2000.

Cleaning Agents

The converters are not hermetically sealed. In order to avoid possible damage, any penetration of liquids shall be avoided.

Protection Degree

The DC-DC converters correspond to protection degree IP 40, provided that the female connector is fitted to the converter.

Railway Application

The P Series converters have been designed observing the railway standards EN 50155 and EN 50121. All boards are coated with a protective lacquer.

Isolation

The electric strength test is performed in the factory as routine test in accordance with EN 50116 and IEC/EN 60950 and should not be repeated in the field. Power-One will not honor any warranty claims resulting from electric strength field tests.

Table 14: Isolation

Characteristic		Input to case + outputs[1]	Outputs to case	Output to output[4]	Auxiliaries[3] to input	Auxiliaries[3] to case	Auxiliaries[3] to outputs	Unit
Electric strength test	Factory test >1 s	2.1[1]	1.0	0.5	2.1[1]	1.0	0.5	kVDC
	AC test voltage equivalent to actual factory test	1.5	0.7	0.35	1.5	0.7	0.35	kVAC
Insulation resistance		>300[2]	>300[2]	>100	>300[2]	>100	>100	MΩ

[1] In accordance with EN 50116, IEC/EN 60950, subassemblies are pre-tested with 4.2 kVDC.
[2] Tested at 500 VDC
[3] Insulated secondary-referenced auxiliary circuits, i.e., Out OK circuit (option D), secondary inhibit input (option i).
[4] Powertrain with 5.1 and 3.3 V output have a commun return.

Safety of Operator-Accessible Output Circuits

If the output circuit of a DC-DC converter is operator accessible, it shall be an SELV circuit according to the IEC/EN 60950 related safety standards.

The following table shows some possible installation configurations, compliance with which causes the output circuit of the DC-DC converter to be an SELV circuit according to IEC/EN 60950 up to a configured output voltage (sum of nominal voltages if in series or +/– configuration) of 35 V.

However, it is the sole responsibility of the installer to ensure the compliance with the relevant and applicable safety regulations.

Use fuses and earth connections as per table below. See also *Installation Instructions*.

Table 15: Safety concept leading to an SELV output circuit

Conditions	Front end			DC-DC converter	Result
Nominal supply voltage	Minimum required grade of insolation, to be provided by the AC-DC front end, including mains supplied battery charger	Maximum DC output voltage from the front end [1]	Minimum required safety status of the front end output circuit	Measures to achieve the specified safety status of the output circuit	Safety status of the DC-DC converter output circuit
Mains ≤250 VAC	Functional (i.e. there is no need for electrical isolation between the mains supply circuit and the DC-DC converter input circuit)	≤168 V	Primary circuit (The nominal voltage between any input pin and earth shall not exceed 250 VAC or 240 VDC.)	Double or reinforced insulation, based on 250 VAC and 240 VDC (provided by the DC-DC converter) and earthed case [2]	SELV circuit
	Basic		Earth related hazardous voltage secondary circuit (The nominal voltage between any input pin and earth shall not exceed 250 VAC or 240 VDC.)	Double or reinforced insulation, based on the maximum nominal output voltage from the front end (both provided by the DC-DC converter) and earthed case [2]	
			Unearthed hazardous voltage secondary circuit	Supplementary insulation, based on 250 VAC and DC and double or reinforced insulation, based on the maximum nominal output voltage from the front end (both provided by the DC-DC converter) and earthed case [2]	
	Supplementary		Unearthed hazardous voltage secondary circuit [3]	Basic insulation, based on 250 VAC and DC (provided by the DC-DC converter)	

[1] The front end output voltage should match the specified input voltage range of the DC-DC converter. The maximum rated input voltage of EP types is 150 V according to IEC/EN 60950.

[2] The earth connection has to be procided by the installer according to the relevant safety standards, e.g., IEC/EN 60950.

[3] Has to be insulated from earth by at least supplementary insulation (by the installer) according to the relevant safety standards, e.g. IEC/EN 60950, based on the maximum nominal output voltage from the front end. If the converter case is accessible, it has to be earthed or the front end output circuit has to be insulated from the converter case by at least basic insulation, based on the maximum nominal mains supply voltage.

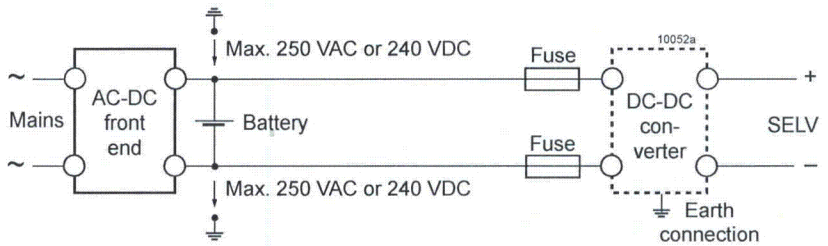


Fig. 24
Schematic safety concept

Description of Options

Option D: Out OK Monitor

Option D monitors the state of the output error amplifiers on both power trains and not the input voltage, output voltage or the current limit. It signals a fault, when one of the error amplifiers reaches its limit, which means that at least one output voltage is not within its regulation limits. This could be because the input voltage is below the minimum level or the load current is too high. This function is not adjustable.

A galvanically isolated open-collector output generates the "Out OK" signal. The circuit monitors simultaneously if

- the input voltage is present - same logic as LED "In OK"
- the output voltages are within their limits - same logic as LED(s) "Out OK".

The open collector is conducting, if the monitored conditions are fulfilled.

This option is located on a subassembly allowing special circuit design on customer request.

Table 16: Output OK data

Characteristics / Conditions		min	typ	max	Unit
V_{OK}	Out OK voltage Output good, I_{OK} < 50 mA		0.8	1.5	V
I_{OK}	Out OK current Output out of range, V_{OK} < 18 V			25	µA

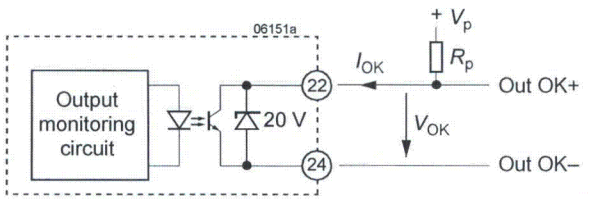


Fig. 25
Output OK circuit (option D)

Dimensioning of resistor value $R_p \geq \frac{V_p}{50\ mA}$

Caution: The Out OK circuit is protected by a Zener diode. To prevent damage, the applied current I_{OK} should be limited to ±50 mA. The Zener diode should not be exposed to more than 0.25 W.

Option T: Active Current Sharing

For 3.3 V and 5.1 V outputs only. The current share facility should be used, where several converters are operated in parallel. Examples could be high reliability n+1 redundant systems or systems providing higher output power.

Using this feature reduces the stress of individual converters and improves the reliability of the system. Interconnection of the current sharing pins T or T1 causes the converters to share their output current evenly.

In redundant systems, the outputs of the converters are decoupled by ORing diodes. Consequently, a failure of one converter will not lead to a system failure.

Since the voltage on the T or T1 pin is referenced to the sense pin S–, the installer must ensure that the S– pins of all parallel converters are at the same electrical potential and that there are no voltage drops across the connection lines between these pins.

BP – GP2000 converters with outputs connected in series can also be paralleled with current sharing, if pins Vo1– of all converters are connected together; see *Sense Lines*. If the output voltages are programmed to a voltage other than $V_{o\ nom}$ by means of the R pin, the outputs should be adjusted individually within a tolerance of ±1%.

Note: Option T is only available for 3.3 V or 5.1 V single-output power trains and only for output 1. In dual- or triple-output models, option T1 influences only output 1. In addition, the second power train has no R input (since no pin is left for that function).

Option i: Secondary-Referenced Inhibit

The inhibit function is located on the primary side. Option i gives the possibility of an inhibit function on the secondary side using two galvanically isolated pins i+ and i–. The power supply may be inhibited from either the input or the output inhibit logic. The inhibit is enabled or disabled by a logic signal (TTL, CMOS, etc). Output enabled: Logic low (<0.8 V) Output inhibited: Logic high (>2.4 V).

This option excludes Opt.-D.

Opt.-i is located on a subassembly allowing special circuit design on customer request.

The secondary inhibit is fully floating with operational insulation to the secondary circuits (which is not sufficient to be used as a primary to secondary insulation).

The input is CMOS compatible, and the level should not exceed 5V. The internal pull-up (to an internal 5 V supply) is 10 kOhms. We suggest connecting i– to Sense–; otherwise the inhibit potential will be undefined.

Option B1 and B3: Heat Sink

The converter is fitted with an additional heat sink.

Table 17: Thermal resistance case to ambient (approx. values)

Option	Thermal resistance	Thickness of case
Standard, 160 mm long	1.6 K/W	< 20 mm
Housing, 220mmlong [1]	1.4 K/W	< 20 mm
Option B1	1.4 K/W	< 40 mm
Option B3	1.2 K/W	< 50 mm

[1] Customer-specific models

Option G

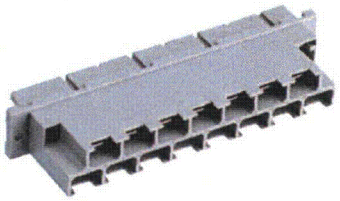
RoHS compliant for all six substances.

Accessories

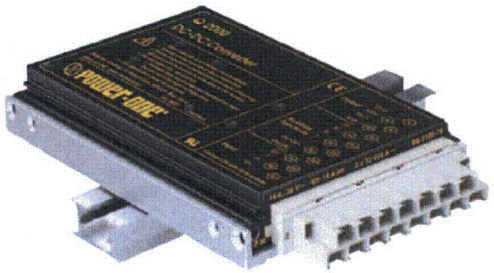
A great variety of electrical and mechanical accessories are available:

- Additional external input or output filters
- Mating connectors including fast-on, screw, solder, or press-fit terminals
- Cable connector housing
- Front panels for 19" rack in 3U or 6U configuration
- Mechanical mounting supports for chassis, DIN-rail, and PCB mounting
- Connector retention facilities

For additional accessory product information, see the accessory data sheets listed with each product series or individual model listing at *www.power-one.com.*



H15 female connector, code key system



Universal mounting bracket for DIN-rail and chassis mounting

Front panel for 19" rack with 6U

EC Declaration of Conformity

CE MARKING

We, **Power-One, Inc.,740 Calle Plano, Camarillo, CA. 93012 USA**
declare under our sole responsibility that the products;

Power Supply Model: P Series

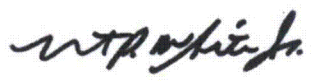
to which this declaration relates, is/are in compliance with the following document(s):

Quality Standard(s): **ISO 9001, EN 29001**

Directive: **DIR 73/23/EEC, Low Voltage Directive**

Product Safety Standard(s): **EN 60950-1: 2001**
IEC 60950-1: 2001
(Licensed by a Notified Body to the European Union)

These component level power supplies are intended exclusively for inclusion within other equipment by an industrial assembly operation or by professional installers per the Installation Instructions provided with the power supplies. The power supplies are considered Class I and must be connected to a reliable earth grounding system.



(Manufacturer)

Camarillo, Ca. *(Place)*

July 5, 2006 *(Date)*

Robert P. White Jr.
Product Safety Director

Ethernet media converter for industrial use

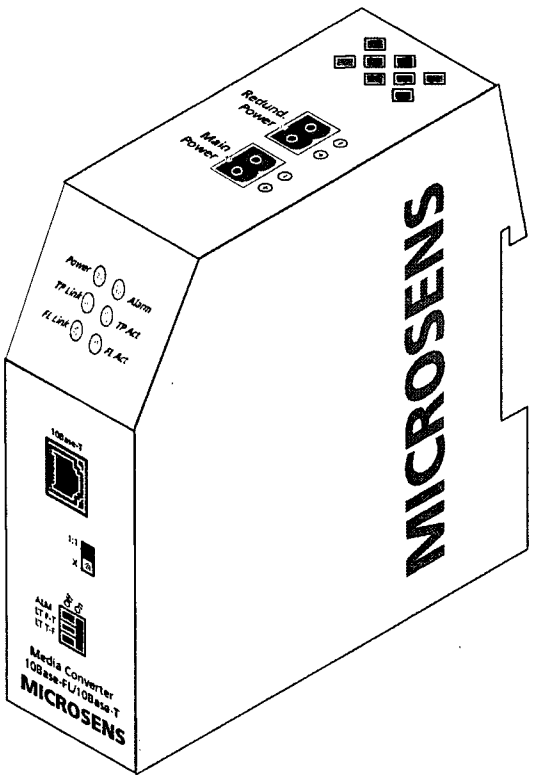
MICROSENS

General

For the extreme demanding use in industrial environments MICROSENS has developed special media converter.

The converter has included several features such as Link Through, ALM, potential free alarm contacts, connector for redundant power supply, cross over switch, solid metal chassis and an extended temperature range.

The industrial product range includes beside the Ethernet (10Base-FL/10Base-T) and Fast Ethernet (100Base-FX/100Base-TX) converter of this data sheet also media converter for serial interfaces (RS-232, RS-422, RS-485).



Technical Specifications

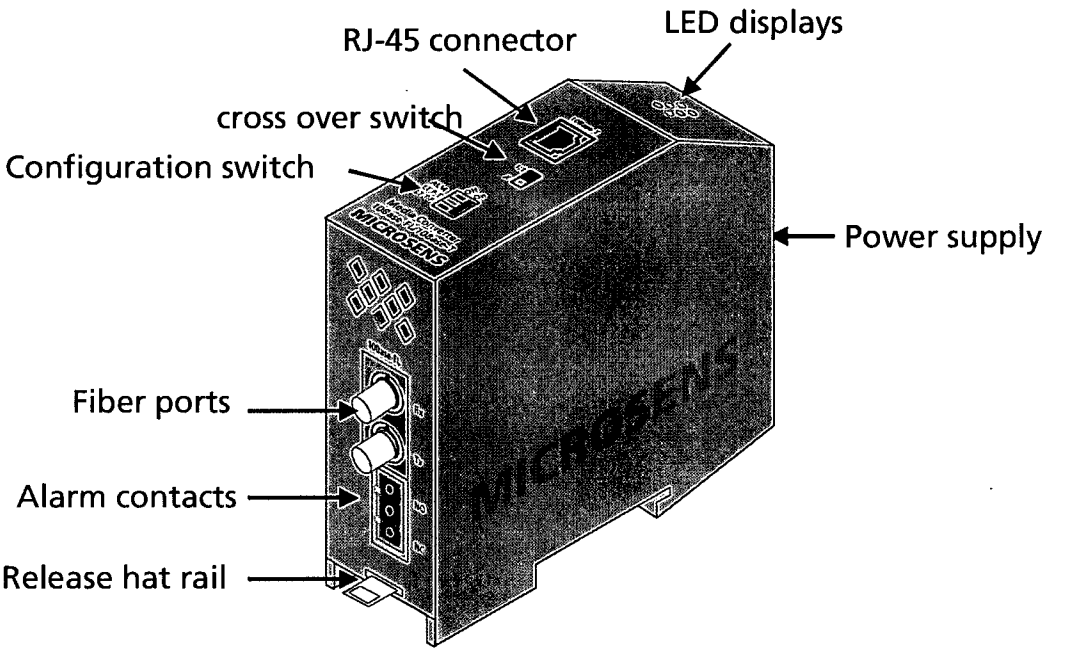
Type	Ethernet / Fast Ethernet media converter for industrial use
Fiber type	Multimode 62,5/125 or 50/125µm, Single mode 9/125µm, duplex
Cable type	Shielded Twisted Pair cable, 100 Ohm, Category 5, Pinout RJ45-port crossable per switch, 100 m
Data rate	10 and 100 Mbit/s
LED displays	*Power* Ready for operation *FX-Link* Fiber link *FX-Act* Data traffic on fiber *TX-Link* Twisted Pair link *TX-Act* Data traffic on Twisted Pair *Alarm* Link interrupted
Mounting	35 mm hat rail, according DIN EN 50 022
Power supply	18 - 36 V DC / max. 500 mA by external power supply Connection by screw terminal, redundant connector
Dimensions	38 x 108 x 116 mm (B x T x H)
Operating temp.	-20°C to 60°C
Storage temp.	-20°C to 80°C
Rel. humidity	5% to 90% non condensing

Optical parameter

Ethernet multimode	*min. distance:*	2 km
	opt. power:	-19 dBm
	sensitivity:	-32,5 dBm
	wavelength:	850 nm
Ethernet single mode	*min. distance:*	10 km (full duplex)
	opt. power:	-24 dBm
	sensitivity:	-32,5 dBm
	wavelength:	1310 nm

Fast Ethernet MM	*min. distance:*	2 km (full duplex)
	opt. power:	-19 dBm
	sensitivity:	-31 dBm
	wavelength:	1310 nm
Fast Ethernet SM	*min. distance:*	15 km (full duplex)
	opt. power:	- 15 dBm
	sensitivity:	- 31 dBm
	wavelength:	1310 nm
	min. distance:	40 km (full duplex)
	opt. power:	- 5 dBm
	sensitivity:	- 34 dBm
	wavelength:	1310 nm
	min. distance:	80 km (full duplex)
	opt. power:	- 5 dBm
	sensitivity:	- 34 dBm
	wavelength:	1550 nm
	min. distance:	125 km (full duplex)
	opt. power:	0 dBm
	sensitivity:	- 37 dBm
	wavelength:	1550 nm

Connectors



Connections

The connection of the media converter to a hub /switch can be done with a standard 1:1 patch cable. Because the pinout of the RJ-45 port can be crossed it is also possible to use a 1:1 patch cable to connect end devices.

Autonegotiation (only for Fast Ethernet version)

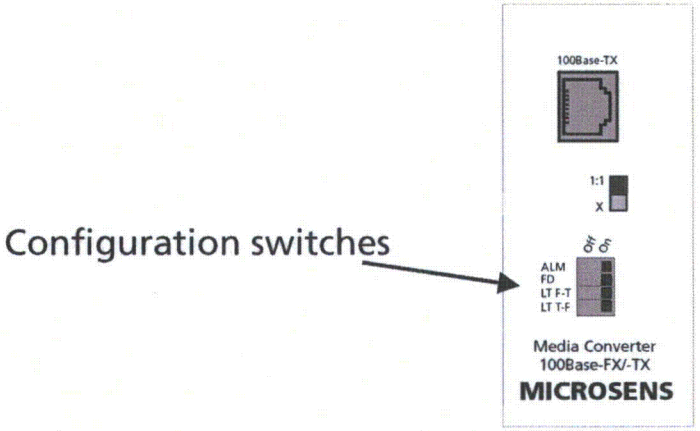
This protocol is used during the connection establishment to recognise the transmission mode (half or full duplex). This ensures that always the maximum transmission speed is reached. Because the autonegotiation protocol is not defined for the fiber side, the converter has a helpful manual configuration feature.

To support the configuration MICROSENS offers this protocol and allows the configuration of the full duplex mode (DIP switch FD: on). Now the converter is getting active during the connection establishment and reacts on the autonegotiation protocol of the connected device.

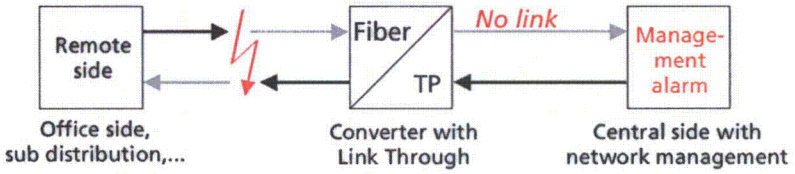
If this feature is deactivated the converter has no effect on the configuration of the connection. The transmission mode half or full duplex is determinated by the connected devices then.

Link Transparency

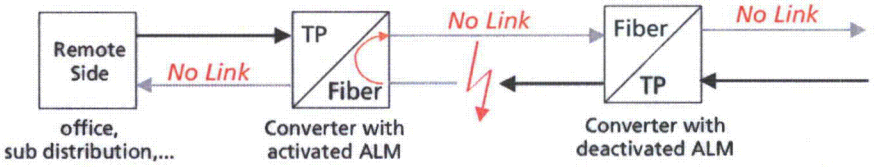
At most of the application the connection states of each segment is monitored by the management of the central switch or hub. Using media converter has the problem that the connection is divided in two different segments. It can happen that an interruption in one segment is not noticed in the other segment. To avoid this problem these media converter have the integrated "Link Through" functionality which is forwarding the link status from one segment to the other.



To ensure that the network management can read the connection status, the converter has additional integrated features such as Link Through and Advanced Link Monitor (ALM). The Link Through forwards the connection status to the converted segment. Due to this the fiber port is interrupted if the twisted pair connection fails and vice versa.



Additional to Link Through the loss of the transmitting optic fiber can be recognized by Advanced Link Monitor (switch ALM FX: on). In case of loss of the fiber port, the copper and the fiber port is switched off (see Fig. 9). This ensures that the central network components can determinate this failure exactly.



Media converter with integrated ALM feature can be combined with all central equipment (e.g. switches, hubs, bridges).

Attention: To ensure the correct setup of the connection, only one side of the connection should have activated ALM.

Alarm relay contacts

The converter has potential free relay contacts for the connection of external alarm systems. The connection is done by a 3 pin screw connector at the bottom of the device. At this connector the pinout, opened or closed (NO/NC), can be selected. This contact is switched in case of loosing a connection (twisted pair and fiber) or a general failure of the device.

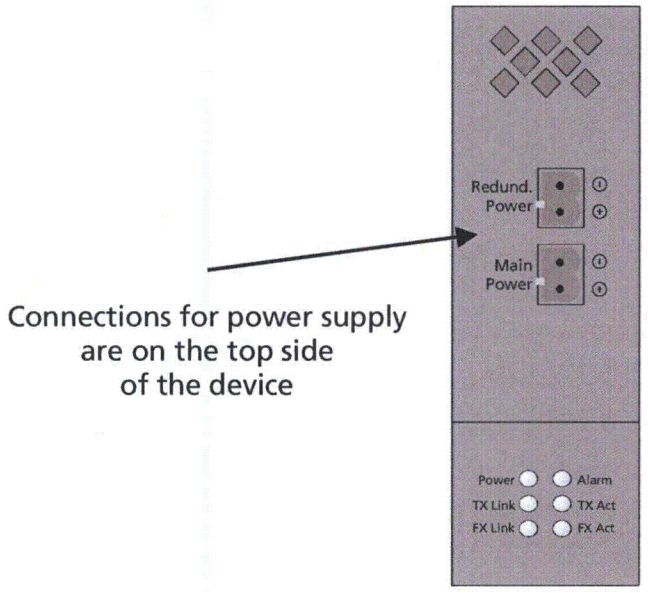
Length reduction (only for Fast Ethernet version)

Half duplex transmission
The converter has a signal delay of max. 25 bit times. Through this, the maximum segment length of 412 m is reduced about 25 m for fiber and about 30 m for twisted pair cable. This reduction has also to be considered at single mode fiber.

Full duplex transmission
In full duplex segments the signal delay has no influence on the maximum segment length.

Power supply

The power is supplied is done by an external power supply unit, which is not included at delivery. The connection is done by plug gable screw terminals at the top of the device. The connection of a redundant power supply is possible with the second terminal.



Mounting

The converter has a very solid metal chassis prepared for the mounting on 35 mm hat rails. The mounting is done on 35 mm hat rails according DIN EN 50 022. The fixation of the MICROSENS switch on the rail is done with a locking pin that can be opened from the bottom side. Multiple devices can be lined up on the rail.

Order designation

Art.-No.	Description	Connectors
MS650400-T	Ethernet media converter 10Base-FL / 10Base-T Multimode 850 nm (Option -T: Link Through can not be switched off!, Funktion on page 5)	2 x ST, 1 xRJ45 Power supply, Relay Contacts
MS650405-T	Ethernet media converter 10Base-FL / 10Base-T Single mode 1300 nm (Option -T: Link Through can not be switched off!, Funktion on page 5)	2 x ST, 1 xRJ45 Power supply, Relay Contacts
MS650420	Fast Ethernet media converter 100Base-FX / 100Base-TX Multimode 1300 nm	2 x SC, 1 xRJ45 Power supply, Relay Contacts
MS650421	Fast Ethernet media converter 100Base-FX / 100Base-TX Multimode 1300 nm	2 x ST, 1 xRJ45 Power supply, Relay Contacts
MS650424	Fast Ethernet media converter 100Base-FX / 100Base-TX Single mode 1300 nm	2 x SC, 1 xRJ45 Power supply, Relay Contacts
MS650425	Fast Ethernet media converter 100Base-FX / 100Base-TX Single mode 1300 nm	2 x ST, 1 xRJ45 Power supply, Relay Contacts
MS650426	Fast Ethernet media converter 100Base-FX / 100Base-TX Single mode 1300 nm, 40 km	2 x SC, 1 xRJ45 Power supply, Relay Contacts

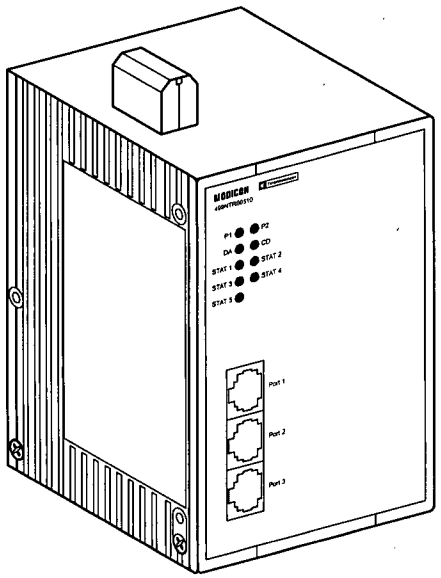
Schneider Electric

ETHERNET CABLING SYSTEM

Quick Reference Guide

ETHERNET HUB 10 Mbps 3TP/2FL Ethernet Twisted Pair Industrial Hub for ISO/DIN Rail

Order No.
499NOH10510



The Ethernet Hub 10 Mbps 3TP/2FL for ISO/DIN rail allows Ethernet networks to be flexibly constructed in accordance with IEEE standard 802.3 using fiber optic (F/O) and copper technology. The hubs for ISO/DIN rail provide several connection options in one device and are plugged onto the ISO/DIN rail.

The hub has three twisted pair (TP) interfaces and two BFOC optical interfaces. It is possible to connect up to three terminals or other TP segments using Shielded and Foiled Twisted Pair cords (SFTP) in industrial environments with electromagnetic interference.

The F/O parts can be used to connect up to two more terminals or optical network components: an optical ring architecture for example.

The module conforms to the specifications of ISO/IEC standard 8802-3.

You will find a detailed description for construction of a local area network on network design and network installation in the "Transparent Factory User and Planning Guide" (Order no. 490USE13300).

Merlin Gerin
Modicon
Square D
Telemecanique

We have checked that the contents of the technical publication agree with the hardware and software described. However, it is not possible to rule out deviations completely, so we are unable to guarantee complete agreement. However, the details in the technical publication are checked regularly. Any corrections which prove necessary are contained in subsequent editions.

We are grateful for suggestions for improvement.

We reserve the right to make technical modifications.

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Note

We would point out that the content of these operating instructions is not part of, nor is it intended to amend an earlier or existing agreement, permit or legal relationship. All obligations on Schneider Automation arise from the respective purchasing agreement which also contains the full warranty conditions which have sole applicability. These contractual warranty conditions are neither extended nor restricted by comments in these operating instructions.

We would furthermore point out that for reasons of simplicity, these operating instructions cannot describe every conceivable problem associated with the use of this equipment. Should you require further information or should particular problems occur which are not treated in sufficient detail in the operating instructions, you can request the necessary information from your Schneider Electric regional sales office.

General

Electricity is used to operate this equipment. Comply in every detail with the safety requirements specified in the operating instructions regarding the voltages to apply!

Warning
If warning notes are ignored, severe injuries and/or material damage may occur.

Only appropriately qualified staff should work on or near this equipment. Such staff must be thoroughly acquainted with all the warnings and maintenance measures contained in these operating instructions.

The proper and safe operation of this equipment assumes proper transport, appropriate storage and assembly and careful operation and maintenance.

Staff qualification requirements

Qualified staff within the meaning of these operating instructions or the warning notes are persons familiar with setting up, assembling, starting up and operating this product and who have appropriate qualifications to cover their activities, such as:

- training or instruction/entitlement to switch circuits and equipment/systems on and off, ground them and identify them in accordance with current safety standards;
- training or instruction in accordance with current safety standards in looking after and using appropriate safety equipment;
- first aid training.

Safety guidelines

Warning
Ethernet Hub 10 Mbps 3TP/2FL units are designed for operation with safe extra-low voltage. Accordingly, only safe extra-low voltages (SELV) conforming to IEC950/EN60950/VDE0805 may be connected to the supply voltage connections.

1. Functional description

1.1 GENERAL FUNCTIONS

Signal regeneration
The Hub 10 Mbps 3TP/2FL processes the signal shape and amplitude of the data received.

Retiming
In order to prevent jitter increasing over several segments, the Hub 10 Mbps 3TP/2FL retimes the data to be transmitted.

Preamble regeneration
The Hub 10 Mbps 3TP/2FL supplements lost preamble bits from data received to 64 bits (incl. the start of frame delimiter (SFD)).

Fragment extension
Collisions can cause short fragments to occur. If the Hub 10 Mbps 3TP/2FL receives a fragment, this is supplemented to give the minimum length of 96 bits. This ensures reliable collision detection by all network participants.

Collision handling
If the Hub 10 Mbps 3TP/2FL detects a data collision, it interrupts the transmission. For the duration of the collision, the collided data package is replaced by a jam signal to ensure collision detection by the terminal equipment.

Auto partitioning
Network failures can be caused by permanent occupancy, ruptured lines, lack of terminating resistors, damaged cable insulation and frequent collisions due to electromagnetic interference. In order to protect the network from such failures, the Hub 10 Mbps 3TP/2FL in this case separates the segment in the receiving direction from the rest of the network.
The Hub 10 Mbps 3TP/2FL has this auto partitioning function individually at each port. The other ports can thus continue to be operated without interference if one of the ports has been auto partitioned. In the event of auto partitioning, transmission continues into the TP segment or the F/O line but reception at this port is blocked.

With twisted pair, auto partitioning is activated if
- a data collision lasts longer than 105 µs or
- there are more than 64 consecutive data collisions.

With F/O, auto partitioning becomes active when
- a data collision lasts longer than 1.5 ms (normal mode) or 0.2 ms (redundant mode) or
- there are more than 64 (normal mode) or 16 (redundant mode) consecutive data collisions.

Reconnection
The segment is reconnected to the network as soon as a package with the minimum length of 51 µs is received without collision at the relevant port, i. e. when the segment is working properly again.
When the redundant mode is active, packages >51 µs sent at a F/O port without collision also lead to reconnection.

Jabber control
Due to a defective transceiver or LAN controller, for example, the network can be continuously occupied with data. To protect against this, the Hub 10 Mbps 3TP/2FL interrupts reception
- at the affected TP or AUI port after 5.5 ms. 9.6 µs after the end of the error the auto partitioning will be cancelled. (jabber lockup protection)
- at the relevant F/O port after 3.9 ms. 420 ms after the end of the error the auto partitioning will be cancelled. (Rx jabber)

1.2 SPECIFIC FUNCTIONS OF THE TP INTERFACE

Link control
The Hub 10 Mbps 3TP/2FL monitors the connected TP line segments for short-circuit or interrupt using idle signals during frame pauses in accordance with IEEE standard 802.3 10BASE-T. The Hub 10 Mbps 3TP/2FL does not transmit any data in a TP segment from which it does not receive an idle signals.

Note: A non-occupied interface is assessed as a line interrupt. The TP line to terminal equipment which is switched off is likewise assessed as a line interrupt as the de-energised transceiver cannot transmit idle signals.

Auto polarity exchange
If the reception line pair is incorrectly connected (RD+ and RD- switched) polarity is automatically reversed.

1.3 SPECIFIC FUNCTIONS OF THE F/O INTERFACE

Link control
The Hub 10 Mbps 3TP/2FL monitors the connected F/O lines for interrupts using idle signals during frame pauses in accordance with IEEE standard 802.3 10BASE-FL. The Hub 10 Mbps 3TP/2FL transmits no data to an F/O line from which it is receiving no idle signal.

Redundancy
In areas where data security has top priority, it is possible with the aid of the redundancy function to bridge any failure of an F/O line or Hub 10 Mbps 3TP/2FL. To do so, a replacement line is frequently routed in a different cable run. In the event of a fault, there is an automatic switch between the main line and the replacement. A cross-link within the bus structure creates a ring (see Fig. 5). If any Hub 10 Mbps 3TP/2FL link or Hub 10 Mbps 3TP/2FL fails, every other Hub 10 Mbps 3TP/2FL can still be reached with the aid of the redundant run.

1.4 DISPLAY ELEMENTS

Equipment status
The 4 LEDs on top provide information about the status which affects the function of the entire Hub 10 Mbps 3TP/2FL.

P1 - Power 1 (green LED)
- lit: supply voltage 1 present
- not lit: - supply voltage 1 not present,
  - hardware fault in Hub 10 Mbps 3TP/2FL

P2 - Power 2 (green LED)
- lit: supply voltage 2 present
- not lit: - supply voltage 2 not present,
  - hardware fault in Hub 10 Mbps 3TP/2FL

DA - Data (yellow LED)
- lit: Hub 10 Mbps 3TP/2FL receiving data at at least one interface
- not lit: - Hub 10 Mbps 3TP/2FL not receiving data at any interface,
  - hardware fault in Hub 10 Mbps 3TP/2FL

Depending on network load, the illumination of the LED can vary between flickering to permanent illumination.

CD - Collision Detect (red LED)
- lit: data collision detected at Hub 10 Mbps 3TP/2FL level
- not lit: - no data collision at Hub 10 Mbps 3TP/2FL level

Port Status
These groups of LEDs display port-related information.

LS1 to LS3 - link status of the TP ports (3 x green LED)
- lit: Hub 10 Mbps 3TP/2FL receiving idle signals from TP segment,
  - the TP segment connected is working properly
- not lit: Hub 10 Mbps 3TP/2FL is not receiving any idle signals from TP segment,
  - the assigned TP port is not connected,
  - the equipment connected is switched off,
  - the TP line is interrupted or short-circuited

LS4 - link status of F/O port 4 (green LED)
- lit: Hub 10 Mbps 3TP/2FL receiving idle signals from F/O segment,
  - the F/O segment connected is working properly
- flashes 2 times per period: port has auto partitioned
- not lit: Hub 10 Mbps 3TP/2FL not receiving any idle signals from F/O segment,
  - the assigned F/O port is not connected,
  - the equipment connected is switched off,
  - the F/O receiving fibre is interrupted

LS5 - Link status of F/O port 5 (green LED)
Normal mode switched on
- lit: Hub 10 Mbps 3TP/2FL receiving idle signals from F/O segment,
  - the connected redundant F/O segment is working properly
- flashes 2 times per period: port has auto partitioned
- not lit: Hub 10 Mbps 3TP/2FL not receiving any idle signals from F/O segment,
  - the assigned F/O port is not connected,
  - the equipment connected is switched off,
  - the F/O receiving fibre is interrupted

LS5 - Link status of F/O port 5 (green LED)
Redundant mode switched on
- lit: Hub 10 Mbps 3TP/2FL receiving idle signals from F/O segment,
  - the connected redundant F/O segment is working properly **and** is active,
- flashes 1 time per period: Hub 10 Mbps 3TP/2FL receiving idle signals from F/O segment,
  - the connected redundant F/O segment is working properly **and** is in stand-by mode,
- not lit: Hub 10 Mbps 3TP/2FL not receiving any idle signals from F/O segment,
  - the assigned F/O port is not connected,
  - the equipment connected is switched off,
  - the F/O receiving fibre is interrupted.

1.5 CONTROLS

6-pin DIP switch

Using the 6-pin DIP switch on the top of the Hub 10 Mbps 3TP/2FL housing

- the message about the link statuses can be suppressed by the indicator contact on a port-by-port basis. Using switches LA1 to LA5, the message about the link status of ports 1 to 5 is suppressed. State on delivery: switch position 1 (ON), i.e. message not suppressed.
- port 5 can be switched to redundant mode. State on delivery: switch position 0 (OFF), i.e. port 5 in normal mode.

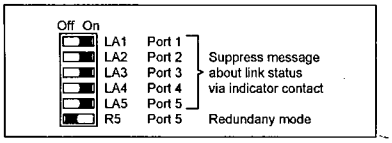

Fig. 1: 6-pin DIP switch

1.6 INTERFACES

TP connection

Three 8 pole RJ45 sockets enable three independent TP segments to be connected.

- **Pin configuration** of the RJ45 socket:
  - TD+: Pin 3, TD-: Pin 6
  - RD+: Pin 1, RD-: Pin 2
  - remaining pins: not configured.

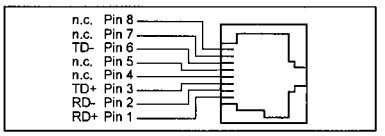

Fig. 2: Pin configuration TP interface

F/O connection

2 optical ports to 10BASE-FL (BFOC/2.5 (ST) sockets) enable Hub 10 Mbps 3TP/2FL equipment to be cascaded as well as redundant rings to be constructed using F/Os and terminal equipment to be connected.

5-pin terminal block

The supply voltage and the indicator contact are connected via a 5-pin terminal block with screw locking mechanism.

Warning

The Hub 10 Mbps 3TP/2FL equipment is designed for operation with SELV. Only safe extra-low voltages to IEC950/EN60950/VDE0805 may therefore be connected to the supply voltage connections and to the indicator contact.

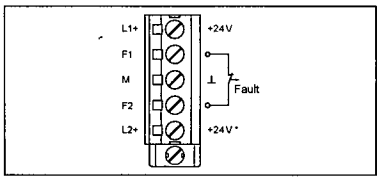

Fig. 3: Pin configuration of 5-pin terminal block

- **Voltage supply**: The voltage supply can be connected to be redundant. Both inputs are decoupled. There is no load distribution. With redundant supply, the power pack only supplies the Hub 10 Mbps 3TP/2FL with the higher output voltage. The supply voltage is electrically isolated from the housing.
- **Indicator contact:** Contact interrupt indicates the following by means of a volt-free indicator contact (relay contact, closed circuit):
  - the failure of at least one of the two supply voltages.
  - a permanent fault in the hub (internal 5 V DC voltage, supply voltage 1 or 2 not in the permissible range).
  - the faulty link status of at least one F/O or TP port.
    The indication of the link state may be masked on a port-by-port basis using DIP switches.
  - at least one port has auto partitioned.
    Port 5 in redundant mode doesn't indicate the state "auto partitioning", because this function characterizes the error free state of the optical ring.

Note: In the case of the voltage supply being routed without redundancy, the Hub 10 Mbps 3TP/2FL indicates the failure of a supply voltage. You can prevent this message by feeding in the supply voltage through both inputs.

2. Configuration

2.1 LINE STRUCTURE

The Hub 10 Mbps 3TP/2FL enables line structures to be built up. Cascading can be effected using both the TP and F/O ports.

2.2 REDUNDANT RING STRUCTURE

Redundant ring structures can be built up using the F/O ports of the Hub 10 Mbps 3TP/2FL. Figure 4 shows a redundant ring structure with Hub 10 Mbps 3TP/2FL equipment. To do so, the first device is connected to the last in the fiber optical line structure which includes Hub 10 Mbps 3TP/2FL equipment (see above) and the redundant fiber optical ring thus closed.

To do so, the redundant connection on just one of the two Hub 10 Mbps 3TP/2FL modules is to be connected to port 5, and port 5 switched to redundant mode. Switchover is effected at the 6-pin DIP switch on top of the equipment (see chapter entitled "Functional description - Controls").

The number of devices which can be cascaded depends on the overall network structure. Redundant ring structures can be implemented via the F/O ports.

Hints on calculating the maximum network expansion can be found in the "Ethernet Reference Manual".

A maximum of 11 Hub 10 Mbps 3TP/2FL modules can be cascaded in a fiber optical line. Here the total length of the line between the terminal devices at each end of the line may not exceed 1180 m.
The total length of the line is determined by the total sum of all F/O line sections and the two TP lines to the terminal devices.

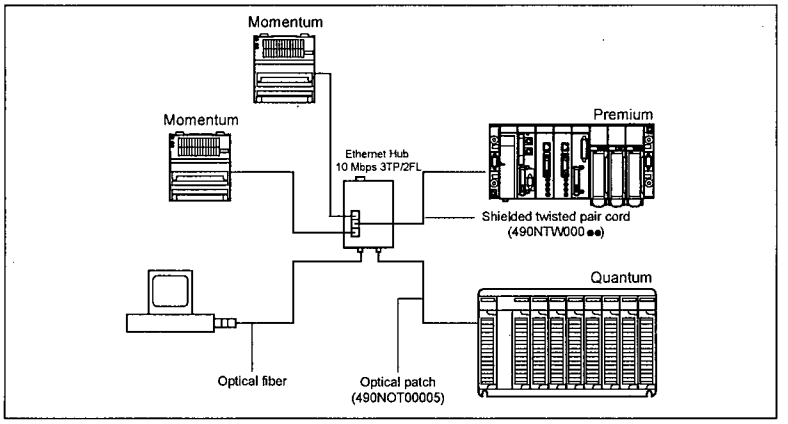

Fig. 4: Standalone configuration of the Hub 10 Mbps 3TP/2FL

When cascading via TP ports, use a cable which crosses the signal pairs, i.e. in each case connects output to input.

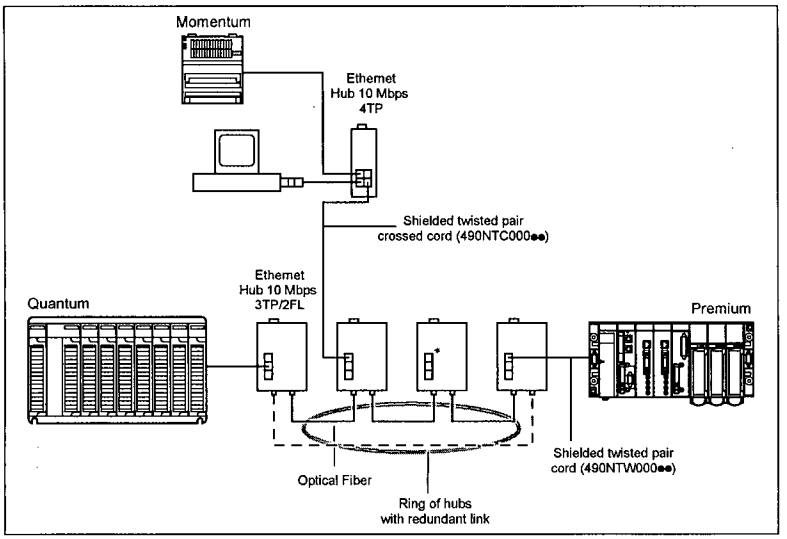

Fig. 5: Redundant ring structure via the F/O ports of the Hub 10 Mbps 3TP/2FL

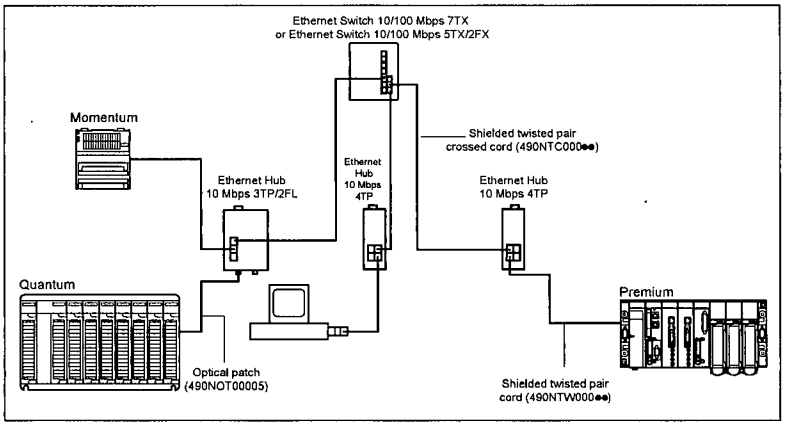

Fig. 6: Configuration with Ethernet switch

3. Assembly, startup procedure and dismantling

3.1 UNPACKING, CHECKING

- Check whether the package was delivered complete (see scope of delivery).
- Check the individual parts for transport damage.

Warning
Use only undamaged parts!

3.2 ASSEMBLY

The equipment is delivered in a ready-to-operate condition. The following procedure is appropriate for assembly:

- Check whether the switch factory-setting is suitable for your requirements.
- Pull the terminal block off the Hub 10 Mbps 3TP/2FL and wire up the supply voltage and indicator lines.
- Fit the Hub 10 Mbps 3TP/2FL on a 35 mm ISO/DIN rail to DIN EN 50 022.
- Suspend the upper snap-on slide bar of the Hub 10 Mbps 3TP/2FL in the standard bar and press it down towards the standard bar until it locks in position.
- Fit the signal lines.

Notes:

- The housing of the Hub 10 Mbps 3TP/2FL is grounded via the ISO/DIN rail. There is no separate ground connection.
- The screws in the lateral half-shells of the housing may not be undone under any circumstances.
- The shielding ground of the twisted pair lines which can be connected is electrically connected to the housing.

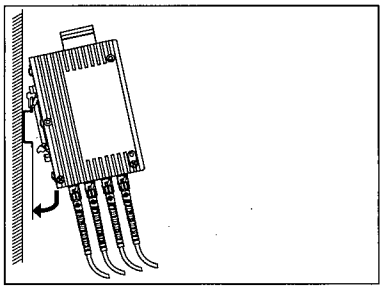

Fig. 7: Assembling the Hub 10 Mbps 3TP/2FL

3.3 STARTUP PROCEDURE

To start up the Hub 10 Mbps 3TP/2FL, connect the supply voltage via the 5-pin terminal block. Lock the terminal block with the locking screw at the side.

3.4 DISMANTLING

To dismantle the Hub 10 Mbps 3TP/2FL from the standard bar, pull the Hub 10 Mbps 3TP/2FL downwards and on the bottom lift the Hub 10 Mbps 3TP/2FL away from the standard bar.

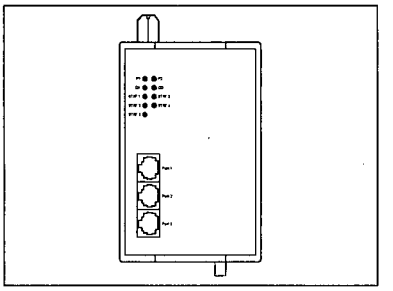

Fig. 8: Dismantling the Hub 10 Mbps 3TP/2FL

4. Technical data

General data

Operating voltage	DC 18 to 32 V safe extra-low voltage (SELV) (redundant inputs decoupled)	
Current consumption	typ. 160 mA at 24 VDC (without data) max. 350 mA at 24 VDC (with data)	
Overload current protection at input	non-changeable thermal fuse	
Dimensions W x H x D	80 mm x 140 mm x 85 mm	(3.15 in x 5.51 in x 3.35 in)
Mass	900 g	(1.982 lb)
Ambient temperature	0 °C to + 60 °C	(32 °F to + 140 °F)
Storage temperature	- 40 °C to + 80 °C	(-40 °F to + 176 °F)
Humidity	10% to 95% (non condensing)	
Protection class	IP 30	
Laser protection	Class 1 conform to EN 60825	
Radio interference level Interference immunity	EN 55022 Class B EN 61000-6-2:1999	
Agency Approval	IEC 61131-2, Marine (Germanisher Lloyd)	

Network size

Transition	TP-Port	TP-Port	F/O port	F/O port
Propagation equivalent	190 m	(623 ft)	260 m	(853 ft)
Variability value	3 BT		3 BT	
Transition	TP-Port	F/O port		
Propagation equivalent	360 m	(1.181 ft)		
Variability value	6 BT	(1 BT = 100 ns)		

F/O port		
Optical output power		
Graded-index fiber 50/125 µm (average)	min. -22,0 dBm	max. -16,2 dBm
Graded-index fiber 62,5/125 µm (average)	min. -19,0 dBm	max. -12,4 dBm
Optical input power	min. -33,0 dBm	

TP line length (TP-Port TP-Port)		
Length of a twisted pair segment	max. 100 m	(328 ft)
Number of cascaded hubs (electrical line)	max. 4	
Number of hubs in an Optical ring	max. 11	
F/O line length (example)		
50/125 µm fiber	max. 2.600 m	(8530 ft)
62.5/125 µm fiber	max. 3.100 m	(10170 ft)

Scope of delivery

Ethernet Hub 10 Mbps 3TP/2FL incl.
terminal block for supply voltage
Quick Reference Guide

Order number
Ethernet Hub 10 Mbps 3TP/2FL 490NOH00510

Accessories

Ethernet SFTP cat5RJ45 cords	490NTW000●●
Ethernet SFTP cat5RJ45 crossed cords	490NTC000●●
Ethernet MTRJ/ST 5 m optical patch	490NOT00005

Note: The optical patch is made up of two 62.5/12.5 multi mode glass fiber, used in 1300 nano-meter wavelengths.

Transparent Factory User and Planning Guide	490USE13300
Transparent Factory Network Design and Cabling Guide	490USE13400

CE **Notes on CE identification**
The devices comply with the regulations of the following European directive:

89/336/EEC
Council Directive on the harmonisation of the legal regulations of member states on electromagnetic compatibility (amended by Directives 91/263/EEC,

Area used	Requirements for emitted interference	interference immunity
Industrial	EN 50081-2: 1993 EN 55022 Class A: 1998	EN 61000-6-2:1999

The product can be used in the residential sphere (residential sphere, business and trade sphere and small companies) and in the industrial sphere.

The precondition for compliance with EMC limit values is strict adherence to the construction guidelines specified in this description and operating instructions.

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Printed in Germany

Schneider Electric

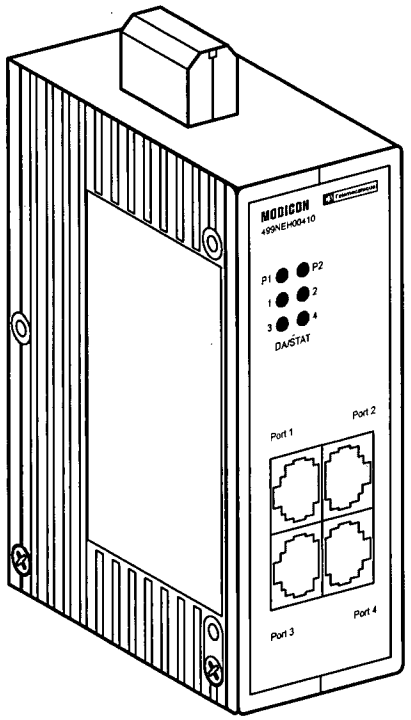
ETHERNET CABLING SYSTEM

Quick Reference Guide

ETHERNET HUB 10 Mbps 4TP
Ethernet Twisted Pair Industrial
Hub for ISO/DIN Rail

Order No.

499NEH10410



The Ethernet hub 10 Mbps 4TP supports fast network expansion. You can connect up to four data terminal devices or further twisted pair segments via shielded twisted pair cords.

To install, just fit the rail hub on an ISO/DIN rail. No other configuration is required. The 24V voltage is supplied via the terminal block and can be fed redundantly.

The terminal block contains an integrated indicator contact, receiving error and warning messages about the hub which are defined as digital signals. These signals can, for example, be utilized as process messages by a Quantum or Premium PLC. The indicator contact becomes active as soon as disturbances occur in the hubs, such as when a power supply fails or at least one TP port reports a faulty link status or has auto partitioned.

LEDs indicating collisions, link status, segmentation, power and received data are available for diagnostic purposes.

The Ethernet Hub 10 Mbps has four twisted pair (TP) shielded interfaces. It is possible to connect up to four terminals or other TP segments using Shielded and Foiled Twisted Pair cords (SFTP) in industrial environments with electromagnetic interference.

The module conforms to the specifications of ISO/IEC standard 8802-3.

You will find a detailed description for construction of a local area network on network design and network installation in the "Transparent Factory User and Planning Guide" (Order no. 490USE13300).

Merlin Gerin
Modicon
Square D
Telemecanique

We have checked that the contents of the technical publication agree with the hardware and software described. However, it is not possible to rule out deviations completely, so we are unable to guarantee complete agreement. However, the details in the technical publication are checked regularly. Any corrections which prove necessary are contained in subsequent editions.

We are grateful for suggestions for improvement.

We reserve the right to make technical modifications.

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Note

We would point out that the content of these operating instructions is not part of, nor is it intended to amend an earlier or existing agreement, permit or legal relationship. All obligations on Schneider Automation arise from the respective purchasing agreement which also contains the full warranty conditions which have sole applicability. These contractual warranty conditions are neither extended nor restricted by comments in these operating instructions.

We would furthermore point out that for reasons of simplicity, these operating instructions cannot describe every conceivable problem associated with the use of this equipment. Should you require further information or should particular problems occur which are not treated in sufficient detail in the operating instructions, you can request the necessary information from your Schneider Electric regional sales office.

General

Electricity is used to operate this equipment. Comply in every detail with the safety requirements specified in the operating instructions regarding the voltages to apply!

Warning
If warning notes are ignored, severe injuries and/or material damage may occur.

Only appropriately qualified staff should work on or near this equipment. Such staff must be thoroughly acquainted with all the warnings and maintenance measures contained in these operating instructions.

The proper and safe operation of this equipment assumes proper transport, appropriate storage and assembly and careful operation and maintenance.

Staff qualification requirements

Qualified staff within the meaning of these operating instructions or the warning notes are persons familiar with setting up, assembling, starting up and operating this product and who have appropriate qualifications to cover their activities, such as:

- training or instruction/entitlement to switch circuits and equipment/systems on and off, ground them and identify them in accordance with current safety standards;
- training or instruction in accordance with current safety standards in looking after and using appropriate safety equipment;
- first aid training.

Safety guidelines

Warning
Ethernet Hub 10 Mbps 4TP units are designed for operation with safe extra-low voltage. Accordingly, only safe extra-low voltages (SELV) conforming to IEC950/EN60950/VDE0805 may be connected to the supply voltage connections.

1. Functional description

1.1 GENERAL FUNCTIONS

Signal regeneration
The Hub 10 Mbps 4TP processes the signal shape and amplitude of the data received.

Retiming
In order to prevent jitter increasing over several segments, the Hub 10 Mbps 4TP retimes the data to be transmitted.

Preamble regeneration
The Hub 10 Mbps 4TP supplements lost preamble bits from data received to 64 bits (incl. the start of frame delimiter (SFD)).

Fragment extension
Collisions can cause short fragments to occur. If the Hub 10 Mbps 4TP receives a fragment, this is supplemented to give the minimum length of 96 bits. This ensures reliable collision detection by all network participants.

Collision handling
If the Hub 10 Mbps 4TP detects a data collision, it interrupts the transmission. For the duration of the collision, the collided data package is replaced by a jam signal to ensure collision detection by the terminal equipment.

Auto partitioning
Network failures can be caused by permanent occupancy, ruptured lines, lack of terminating resistors, damaged cable insulation and frequent collisions due to electromagnetic interference. In order to protect the network from such failures, the Hub 10 Mbps 4TP in this case separates the segment in the receiving direction from the rest of the network.
The Hub 10 Mbps 4TP has this auto partitioning function individually at each port. The other ports can thus continue to be operated without interference if one of the ports has been auto partitioned. In the event of auto partitioning, transmission continues into the TP segment but reception at this port is blocked.
With twisted pair, auto partitioning is activated if
- a data collision lasts longer than 105 µs or
- there are more than 64 consecutive data collisions.

Reconnection
The segment is reconnected to the network as soon as a package with the minimum length of 51 µs is received without collision at the relevant port, i.e. when the segment is working properly again.

Jabber control
Due to a defective transceiver or LAN controller, for example, the network can be continuously occupied with data. To protect against this, the Hub 10 Mbps 4TP interrupts reception at the affected TP port after 5.5 ms for a duration of 9.6 µs. This cycle (transmission for 5.5 ms, interruption for 9.6 µs) is repeated until the end of the error (jabber lockup protection).

1.2 SPECIFIC FUNCTIONS OF THE TP INTERFACE

Link control
The Hub 10 Mbps 4TP monitors the connected TP line segments for short-circuits or interrupts, using idle signals during frame pauses, in accordance with IEEE standard 802.3 10BASE-T. The Hub 10 Mbps 4TP does not transmit any data in a TP segment from which it does not receive an idle signal.

Note: A non-occupied interface is assessed as a line interrupt. The TP line to terminal equipment which is switched off is likewise assessed as a line interrupt as the de-energized transceiver cannot transmit idle signals.

Auto polarity exchange
If the reception line pair is incorrectly connected (RD+ and RD- switched) polarity is automatically reversed.

1.3 DISPLAY ELEMENTS

Equipment status
The two LEDs provide information about the status which affects the function of the entire Hub 10 Mbps 4TP.

P1 - Power 1 (green LED)
- lit: supply voltage 1 present
- not lit: - supply voltage 1 not present,
  - hardware fault in Hub 10 Mbps 4TP

P2 - Power 2 (green LED)
- lit: supply voltage 2 present
- not lit: - supply voltage 2 not present,
  - hardware fault in Hub 10 Mbps 4TP

Port Status
These groups of LEDs display port-related information.
DA/STAT 1 to DA/STAT 4 - link status of the TP ports (4 x green/yellow LED)
- lit yellow:
Hub 10 Mbps 4TP receiving data
- lit green:
Hub 10 Mbps 4TP receiving link test pulses from TP segment,
- the TP segment connected is working properly
- flashes
  green: port has auto partitioned
- not lit: Hub 10 Mbps 4TP is not receiving any idle signals from TP segment,
  - the assigned TP port is not connected,
  - the equipment connected is switched off,
  - the TP line is interrupted or short-circuited

1.4 CONTROLS

6-pin DIP switch
Using the 6-pin DIP switch on the top of the Hub 10 Mbps 4TP housing
- the message about the link status can be suppressed by the indicator contact on a port-by-port basis. Using switches LA1 to LA4, the message about the link status of ports 1 to 4 is suppressed. Factory setting: switch position 1 (ON), i.e. message not suppressed.

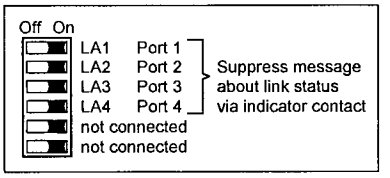


Fig. 1: 6-pin DIP switch

1.5 INTERFACES

TP connection
Four 8 pole RJ45 sockets enable four independent TP segments to be connected.
- **Pin configuration** of the RJ45 socket:
  - TD+: Pin 3, TD-: Pin 6
  - RD+: Pin 1, RD-: Pin 2
  - remaining pins: not configured.

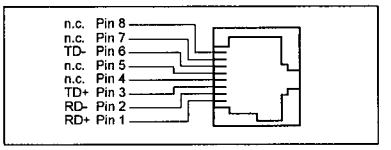


Fig. 2: Pin configuration TP interface

5-pin terminal block
The supply voltage and the indicator contact are connected via a 5-pin terminal block with screw locking mechanism.

Warning
The Hub 10 Mbps 4TP equipment is designed for operation with SELV. Only safe extra-low voltages to IEC950/EN60950/VDE0805 may therefore be connected to the supply voltage connections and to the indicator contact.

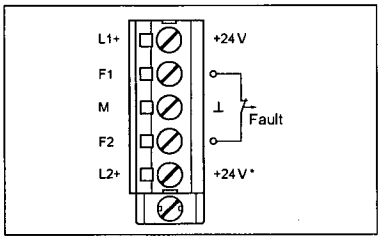


Fig. 3: Pin configuration of 5-pin terminal block

- **Voltage supply**: The voltage supply can be connected to be redundant. Both inputs are decoupled. There is no load distribution. With redundant supply, the power pack only supplies the Hub 10 Mbps 4TP with the higher output voltage. The supply voltage is electrically isolated from the housing.
- **Indicator contact:** Contact interrupt indicates the following by means of a volt-free indicator contact (relay contact, closed circuit):
  - the failure of at least one of the two supply voltages.
  - a permanent fault in the hub (internal 5 V DC voltage, supply voltage 1 or 2 not in the permissible range).
  - the faulty link status of at least one TP port. The indication of the link state can be masked on a port-by-port basis using DIP switches.
  - at least one port has auto partitioned.

Note: In the case of the voltage supply being wired without redundancy, the Hub 10 Mbps 4TP indicates the failure of a supply voltage. You can prevent this message by feeding the supply voltage through both inputs.

2. Configuration

2.1 STANDALONE STRUCTURE STAR SHAPED STRUCTURE

The Hub 10 Mbps 4TP enables connection of up to four data terminal devices or further twisted pair segments via twisted pair.

2.2 EXPANSION OF EXISTING NETWORKS

The Hub 10 Mbps 4TP offers the possibility of expanding your network quickly, for example by using an existing hub / switch link.

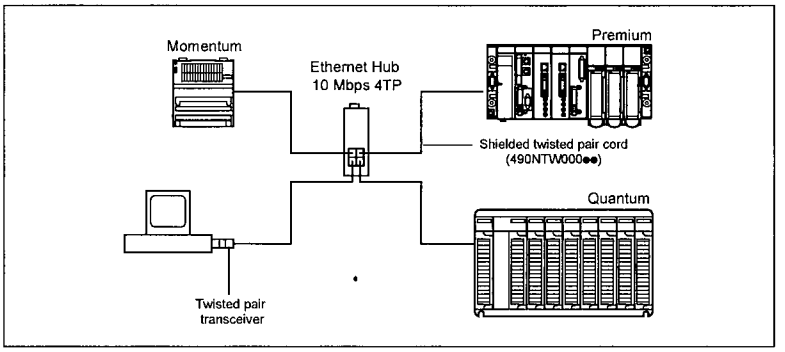


Fig. 4: Standalone configuration of the Hub 10 Mbps 4TP

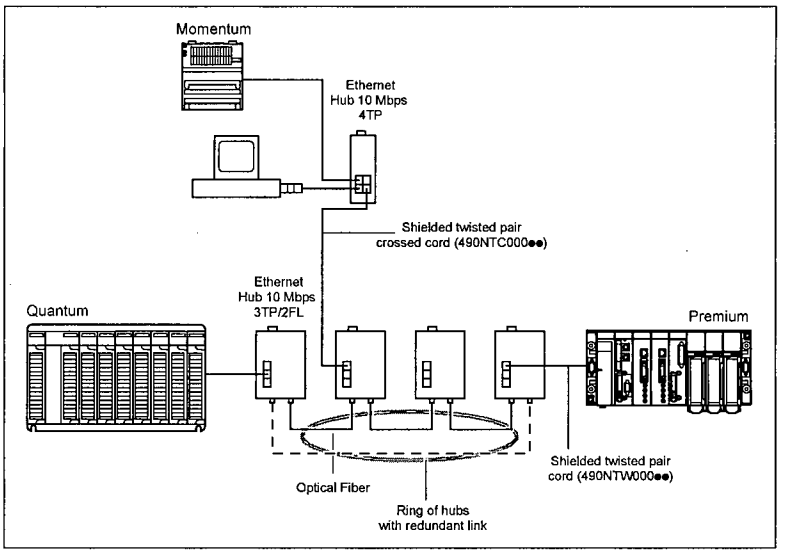


Fig. 5: Expansion of a hub link

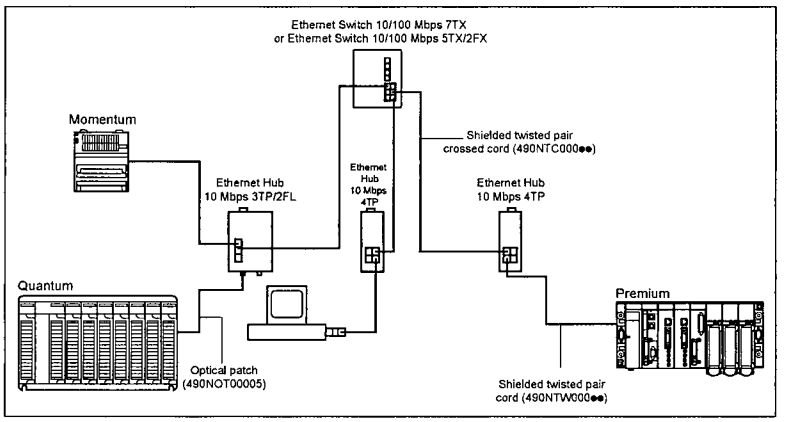


Fig. 6: Configuration with Ethernet switch

3. Assembly, startup procedure and dismantling

3.1 UNPACKING, CHECKING

- Check whether the package was delivered complete (see scope of delivery).
- Check the individual parts for transport damage.

Warning
Use only undamaged parts!

3.2 ASSEMBLY

The equipment is delivered in a ready-to-operate condition. The following procedure is appropriate for assembly:

- Check whether the switch factory-setting is suitable for your requirements.
- Pull the terminal block off the Hub 10 Mbps 4TP and wire up the supply voltage and indicator lines.
- Fit the Hub 10 Mbps 4TP on a 35 mm ISO/DIN rail to DIN EN 50 022.
- Suspend the upper snap-in hook of the Hub 10 Mbps 4TP on the ISO/DIN rail, insert a screwdriver horizontally under the housing into the locking slide pull this downwards (see Fig. 8, dismantling) and press the bottom of the module onto the ISO/ DIN rail until it locks in position (Fig. 7).
- Fit the signal lines.

Notes:

- The housing of the Hub 10 Mbps 4TP is grounded via the ISO/DIN rail. There is no separate ground connection.
- The screws in the lateral half-shells of the housing must not be undone under any circumstances.
- The shielding ground of the twisted pair lines which can be connected is electrically connected to the housing.

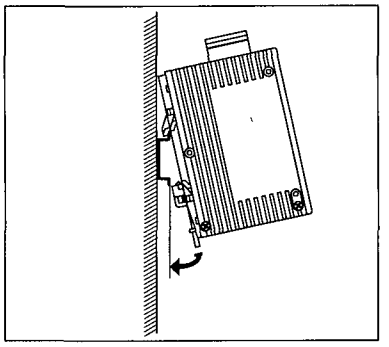


Fig. 7: Assembling the Hub 10 Mbps 4TP

3.3 STARTUP PROCEDURE

You start up the Hub 10 Mbps 4TP by connecting the supply voltage via the 5-pin terminal block. Lock the terminal block with the locking screw at the side.

3.4 DISMANTLING

To take the Hub 10 Mbps 4TP off the ISO/DIN rail, insert a screwdriver horizontally under the housing into the locking slide, pull it (without tipping the screwdriver) downwards and tilt the Hub 10 Mbps 4TP upwards.

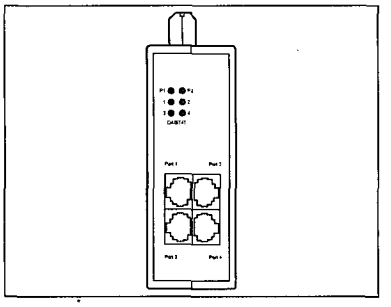


Fig. 8: Dismantling the Hub 10 Mbps 4TP

4. Technical data

General data

Operating voltage	DC 18 to 32 V safe extra-low voltage (SELV) (redundant inputs decoupled)	
Current consumption	typ. 80 mA at 24 VDC (without data) max. 130 mA at 24 VDC (with data)	
Overload current protection at input	non-replaceable thermal fuse	
Dimensions W x H x D	40 mm x 125 mm x 80 mm	(1.57 in x 4.92 in x 3.15 in)
Weight	530 g	(1.167 lb)
Ambient temperature	0 °C to + 60 °C	(32 °F to + 140 °F)
Storage temperature	- 40 °C to + 80 °C	(-40 °F to + 176 °F)
Humidity	10% to 95% (non condensing)	
Protection class	IP 30	
Radio interference level Interference immunity	EN 55022 Class B EN 61000-6-2:1999	
Interfaces	4 ports in compliance to 10BASE-T with RJ45 connectors (shielded) 1 x 5 pole mountable terminal block	
Displays	P1, P2: power DA/STAT 1 to DA/STAT 4: data, collision, link status per port, segmentation	
Agency Approval	IEC 61131-2, Marine (Germanisher Lloyd)	

Network size

Transition	TP-Port TP-Port	
Propagation equivalent	190 m	(624 ft)
Variability value	4 BT	(1 BT = 100 ns)
TP line length (TP-Port TP-Port)		
Length of a twisted pair segment	max. 100 m	(328 ft)
Number of cascaded hubs	max.4	

Scope of delivery

Ethernet Hub 10 Mbps 4TP incl. terminal block for supply voltage Quick reference guide	
Order number Ethernet Hub 10 Mbps 4TP	499NEH10410

Accessories

Ethernet SFTP cat5RJ45 cords	490NTW000●●
Ethernet SFTP cat5RJ45 crossed cords	490NTC000●●
Transparent Factory User and Planning Guide	490USE13300
Transparent Factory Network Design and Cabling Guide	490USE13400

CE **Notes on CE identification**
The devices comply with the regulations of the following European directive:

89/336/EEC
Council Directive on the harmonisation of the legal regulations of member states on electromagnetic compatibility (amended by Directives 91/263/EEC, 92/31/EEC and 93/68/EEC):

Area used	Requirements for emitted interference		interference immunity
Industrial	EN 50081-2: 1993	EN 55022 Class A: 1998	EN 61000-6-2:1999

The product can be used in the residential sphere (residential sphere, business and trade sphere and small companies) and in the industrial sphere.

The precondition for compliance with EMC limit values is strict adherence to the construction guidelines specified in this description and operating instructions.

3500425 0K02000 00

Printed in Germany

FL MC 10/100 BASE-T/FO G1300ST

FO converter for converting 10/100Base-T to multi-mode glass fibers (1300 nm)

INTERFACE

Data sheet
102753_en_02

1 Description

The **FL MC 10/100 BASE-T/FO G1300ST** FO converter provides a high level of immunity to interference and a long transmission range in industrial applications by converting the 10/100Base-T(X) Ethernet interface to fiber optics (100 Mbps according to FX standard).

The supply voltage is 24 V DC. The connection is made either via plug-in screw terminal blocks or via a system power supply unit and T-BUS DIN rail connector. A higher level of availability can be achieved for both versions using a redundant supply.

The auto negotiation function via fiber optics ensures that the maximum possible transmission power is used. In "Transparent" mode, the FO converter behaves like a direct copper connection, which means that the connected devices can negotiate the operating mode automatically.

For easy startup, the FO converter also has an integrated MDI/MDIx changeover. The required line or crossover cable connections can thus be set locally.

The converter also has link monitoring, which separately signals/monitors the operability of the connected cable connection and devices for the twisted pair and fiber optic channels.

If longer distances are to be covered or if an existing glass fiber installation is used, the **FL MC 10/100 BASE-T/FO G1300ST** converter covers distances of up to 10,000 m with 62.5 µm or 6400 m with 50/125 µm multi-mode glass fibers in full duplex mode. The connection conforms to the B-FOC (ST®) standard.

The FO converter conforms to the specifications of standards IEEE 802.3 and ISO/IEC 68802.3.

WARNING: Explosion hazard

The module is designed for use in zone 2, if the specific conditions are observed.

Observe the safety regulations and installation notes on page 4.

If you have any technical problems, which you cannot resolve with the aid of this documentation, please contact us during the usual office hours at:

PSI hotline: +49 - 52 35 - 31 98 90
Fax: +49 - 52 35 - 33 09 99
E-mail: interface-service@phoenixcontact.com

Make sure you always use the latest documentation.
It can be downloaded at www.phoenixcontact.net/download.

This data sheet is valid for all products listed on the following page:

2 Ordering data

FO converter

Description	Type	Order No.	Pcs./Pkt.
FO converter for converting 10/100Base-T(X) to multi-mode glass fibers (1300 nm), DIN rail-mountable, 24 V DC supply	FL MC 10/100 BASE-T/FO G1300ST	2708986	1

Accessories

Description	Type	Order No.	Pcs./Pkt.
Fiber optic glass fiber cable for indoor installation	PSM-LWL-GDM RUGGED-50/125	27 99 32 2	1
Fiber optic glass fiber cable for outdoor installation	PSM-LWL-GDO-50/125	27 99 43 2	1
Heavy CAT5 installation cable	FL CAT5 HEAVY	27 44 81 4	1
Light, flexible CAT5 installation cable	FL CAT5 FLEX	27 44 83 0	1
RJ45 connector, gray for straight cables (2 connectors in the set)	FL PLUG RJ45 GR/2	27 44 85 6	1
RJ45 connector, green for crossed cables (2 connectors in the set)	FL PLUG RJ45 GN/2	27 44 57 1	1
Crimping pliers for RJ45 connectors	FL CRIMPTOOL	27 44 86 9	1
CAT5 connection field, screw terminal block to RJ45	FL CAT5 TERMINAL BOX	27 44 61 0	1

3 Technical data

Ethernet interface	
Ethernet interface	10/100Base-T(X) according to IEEE 802.3u
Connection	RJ45 female connector, shielded
Transmission speed	10/100 Mbps
Auto negotiation modes	Either transparent via TP and FO (default) or locally on TP
Transmission length for TP	100 m (twisted pair, shielded)
Link through	Link down is automatically forwarded to the second connection
MDI/MDIx changeover	Can be switched internally between line (1:1) and crossover connection
Signal LEDs	Activity (yellow LED), link status (green LED), 100 Mbps (green LED)
Cable impedance	100 Ω
Propagation delay (PEV), TP/FO	146 BT (146 m), maximum

Fiber optic interface				
Fiber optic interface	10/100 Mbps (100 Mbps according to FX standard)			
Connection	B-FOC (ST®)			
Wavelength	1300 nm			
Laser protection	Class 1 according to DIN EN 60825-1			
Transmission length including 3 dB system reserve	6400 m glass fiber with F-G 50/125 0.7 dB/km F1200, minimum 2800 m glass fiber with F-G 50/125 1.6 dB/km F800, minimum 10,000 m glass fiber with F-G 62.5/125 0.7 dB/km F1000, minimum 3000 m glass fiber with F-G 62.5/125 2.6 dB/km F600, minimum			
Signal LEDs	Data transmission (yellow LED), link status (green LED)			
Optical output power	**Dynamic (average) in link mode**		**Static**	
Fiber type 50/125 µm	-23.5 dBm, minimum	-14 dBm, maximum	-20.5 dBm, minimum	-11 dBm, maximum
Fiber type 62.5/125 µm	-20 dBm, minimum	-14 dBm, maximum	-17 dBm, minimum	-11 dBm, maximum
Optical receiver sensitivity	-31 dBm, minimum		-28 dBm, minimum	
Overrange	-14 dBm, maximum		-11 dBm, maximum	
MTBF (Mean Time Between Failures) according to Telcordia standard (100% duty cycle)				
At 25°C	500,000 h			
At 40°C	330,000 h			

General data

Supply voltage	24 V DC ±20%
Nominal current consumption	95 mA, maximum
Protection against polarity reversal	Serial diodes
Indicators	UL (green LED)
Connection	Plug-in screw terminal block (COMBICON), redundancy possible
Electrical isolation	10/100Base-T//supply
Test voltage	1500 V_{rms}, 50 Hz, 1 min.
Housing material	PA V0, green
Connection data for screw terminal blocks	0.2 mm^2 ... 2.5 mm^2
Dimensions (W x H x D)	22.5 mm x 99 mm x 127 mm
Weight	120 g
Ambient temperature	
Operation	0°C ... +55°C
Storage/transport	-25°C ... +70°C
Permissible humidity	
Operation	10% ... 95% (no condensation)
Storage/transport	10% ... 95% (no condensation)
Air pressure	
Operation	860 hPa ... 1080 hPa
Storage/transport	660 hPa ... 1080 hPa

Tests/approvals

Ambient compatibility	Free from substances that would hinder coating with paint or varnish according to central standard P-VW-3.10.757 650 of VW, Audi, and Seat
Vibration resistance	EN 60068-2-6, 5g, 1.5 h in xyz direction
Shock test	EN 60068-2-27, storage/transport: 50g, operation: 15g, 11 ms period, half-sine shock pulse
Free fall	1 m
Air and creepage distances	EN 60950-1
ATEX	II 3G Ex nAC IIC T4 X
Approval	File E 140324; Vol. 2, Sec. 3
	File E 199827; Vol. 3, Sec. 4 Cl. 1, Div. 2, Grp. A - D, Temp Code T4A

Conformance with EMC Directive 2004/108/EC and Low Voltage Directive 2006/95/EC

Noise immunity test according to EN 61000-6-2 [P]

Electrostatic discharge (ESD)	EN 61000-4-2	8 kV air discharge [*] 6 kV contact discharge [*]
Electromagnetic HF field	EN 61000-4-3	
Amplitude modulation		10 V/m [¬]
Pulse modulation		10 V/m [¬]
Fast transients (burst)	EN 61000-4-4	
Signal		2 kV/5 kHz [*]
Supply		4 kV/5 kHz [*]
Surge current loads (surge)	EN 61000-4-5	
Signal		2 kV/12 Ω [*]
Supply		0.5 kV/2 Ω [*]
Conducted interference	EN 61000-4-6	10 V [¬]

Noise emission test according to EN 61000-6-4

Noise emission of housing	EN 55011 [+]	Class A [~]

[P] EN 61000 corresponds to IEC 61000
[*] Criterion B: Temporary adverse effects on the operating behavior, which the device corrects automatically.
[¬] Criterion A: Normal operating behavior within the specified limits.
[+] EN 55011 corresponds to CISPR11
[~] Class A: Industrial application, without special installation measures.

4 Safety regulations and installation notes

4.1 Installation and operation

Follow the installation instructions.

NOTE: Installation, operation, and maintenance may only be carried out by qualified specialist personnel.

When installing and operating the device, the applicable safety directives (including national safety directives), accident prevention regulations, as well as general technical regulations must be observed.

NOTE: The circuits inside the device must not be accessed.

Do not repair the device yourself, replace it with an equivalent device. Repairs may only be carried out by the manufacturer.

NOTE: The device is designed to meet IP20 protection when:

- It is installed outside potentially explosive areas.
- The environment is clean and dry.

In order to provide protection against mechanical or electrical damage, install the device in appropriate housing with a suitable degree of protection according to IEC 60529.

NOTE: Operation of the device is only permitted if accessories available from Phoenix Contact are used. The use of other additional components may invalidate the device approval status.

4.2 Safety regulations for installation in potentially explosive areas

For the safety data, please refer to the operating instructions and certificates (EC-type examination certificate, other approvals, if necessary).

Installation in zone 2

WARNING: Explosion hazard
The device is designed for installation in zone 2.

WARNING: Explosion hazard
Devices that are installed in zone 1 must **not** be connected to the fiber optic interface.

Observe the specified conditions for use in potentially explosive areas.

WARNING: Explosion hazard
Install the device in suitable **housing that meets IP54 protection, minimum.**
Observe the requirements of IEC 60079-14/ EN 60079-14, e.g., steel housing with a wall thickness of 3 mm.

WARNING: Explosion hazard
Disconnect the block power supply **before** snapping it on or connecting it.

WARNING: Explosion hazard
Only use category 3G modules (ATEX 94/9/EC).

WARNING: Explosion hazard
Temporary malfunctions (transients) must not exceed the rated voltage by more than 40%.

Installation in areas with a danger of dust explosions

WARNING: Explosion hazard
The device is **not** designed for installation in areas with a danger of dust explosions.

5 Structure

5.1 Example topology

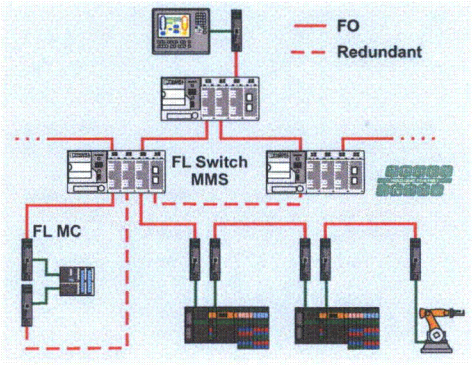


Figure 1 Example topology

5.2 Block diagram

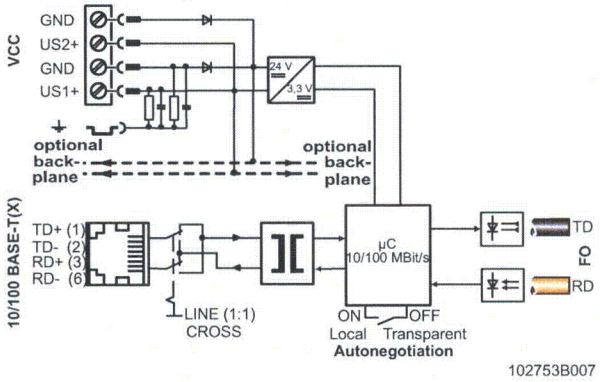


Figure 2 Block diagram

5.3 Function elements

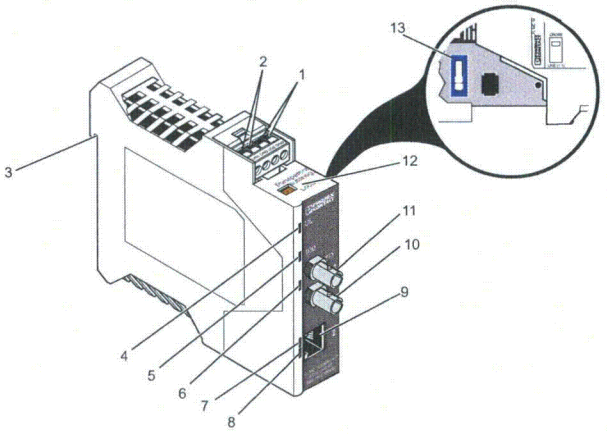


Figure 3 Function elements

1 Redundancy power supply 2 (24 V DC)
2 Power supply 1 (24 V DC)
3 Connection for functional earth ground
4 "UL" LED: Power supply (green)
5 "100" LED: 100 Mbps transmission speed (green)
6 "FO link" LED: Link status of FO port (green)
7 "TP link" LED: Link status of TP port (green)
8 "Activity" LED: Data transmission of TP and FO port (yellow)
9 10/100Base-T(X) connection (TP port)
10 Fiber optic connection, receiver
11 Fiber optic connection, transmitter
12 Local/transparent auto negotiation
13 MDI/MDIx changeover

Housing dimensions

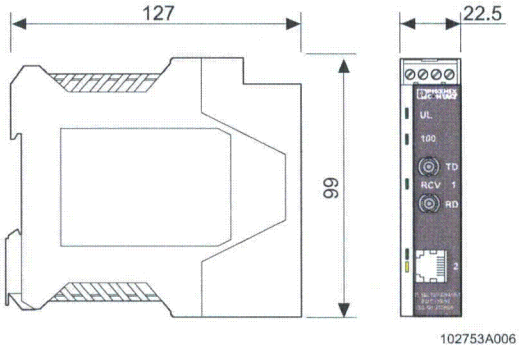


Figure 4 Housing dimensions (in mm)

6 Assembly

6.1 Connection notes

WARNING: Risk of injury and damage to equipment

Only mount and remove modules when the power supply is disconnected.

WARNING: Only suitable for SELV operation

The FL MC 10/100 BASE-T/FO G1300ST is designed exclusively for SELV operation according to IEC 60950/EN 60950/VDE 0805.

NOTE: Electrostatic discharge

The device contains components that can be damaged or destroyed by electrostatic discharge. When handling the device, observe the necessary safety precautions against electrostatic discharge (ESD) according to EN 61340-5-1 and EN 61340-5-2.

Assembly in potentially explosive areas

WARNING: Explosion hazard

Observe the safety notes on page 4.

6.2 Mounting on the DIN rail

- Install the FL MC 10/100 BASE-T/FO G1300ST on a 35 mm DIN rail according to DIN EN 60715.

To avoid contact resistance only use clean, corrosion-free DIN rails. End clamps can be mounted on both sides of the module to stop the modules from slipping on the DIN rail.

WARNING: Ground the module properly

Connect the DIN rail to protective earth ground using a grounding terminal block. The modules are grounded when they are snapped onto the DIN rail. This ensures that the shield is effective. Connect protective earth ground with low impedance.

6.3 Combined assembly with a system power supply unit

1. Connect together the required number of DIN rail connectors for the connection station. One ME 22,5 TBUS 1,5/ 5-ST-3,81 G DIN rail connector is required for each device (Order No. 2707437, see A in Figure 5).
2. Push the connected DIN rail connectors onto the DIN rail (B and C).

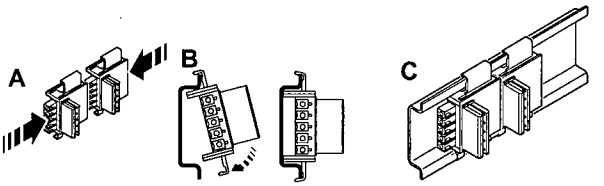


Figure 5 Combined assembly

6.4 Assembly in the control cabinet

1. Install an end clamp next to the left-hand module to prevent the modules from slipping.
2. Place the module onto the DIN rail from above. The upper holding keyway must be hooked onto the top edge of the DIN rail (Figure 6).
3. Push the module from the front towards the mounting surface.
4. Once the module has been snapped on properly, check that it is fixed securely on the DIN rail.
5. Snap the other modules that are to be contacted onto the DIN rail next to one another.

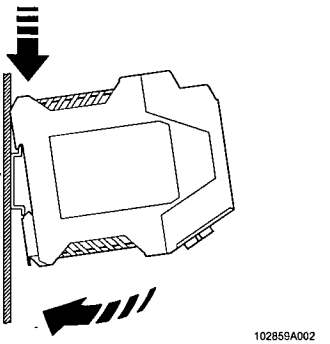


Figure 6 Assembly in the control cabinet

6.5 Removal

1. Pull the locking latch down using a screwdriver, needle-nose pliers or similar.
2. Pull the bottom edge of the module away from the mounting surface.
3. Pull the module diagonally upwards away from the DIN rail.

7 Mode selector switch

Modern Ethernet devices support the auto negotiation mechanism. The devices request the operating mode from one another (half or full duplex mode). If the partner device does not respond to the request, then the requesting device selects half duplex mode. This considerably reduces the maximum achievable distance. If the mode is not the same – half duplex (HD) on one side, full duplex (FD) on the other side – the communication is aborted by a transmission error.

This behavior often occurs when media converters are used, because in the past the auto negotiation signals could not be transmitted via the fiber optic path. As a result, auto negotiation devices select half duplex mode for safety reasons, even if the partner device operates in full duplex mode.

The FL MC 10/100 BASE-T/FO G1300ST offers a remedy in the form of a mechanism, which either transmits the auto negotiation signals via the fiber optic path (transparent) or responds to the requesting device (local) and thus forces full duplex mode.

The mode selector switch is located next to the power supply connection.

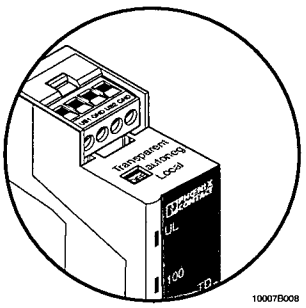


Figure 7 Mode selector switch

The operating mode must be selected before connecting the supply voltage. The changeover only takes effect after power up.

- **Transparent auto negotiation** (default)
  The connected termination devices negotiate the transmission speed (10/100 Mbps) and transmission mode (half/full duplex) directly.
- **Local**
  The transmission speed (10/100 Mbps) is set to the maximum possible value and the transmission mode (half/full duplex) is negotiated separately after each subsection. This mode enables paths, which have a device without auto negotiation on one side, to operate in full duplex mode.

Ensure that the same transmission mode/speed has been selected for all the connected devices.

7.1 Selecting local/transparent auto negotiation

The following settings arise from the possible device combinations:

Termination device 1	Media converter 1	Media converter 2	Termination device 2
Auto negotiation	Transparent (default)		Auto negotiation
100 Mbps full duplex	Transparent (default)		100 Mbps full duplex
100 Mbps half duplex	Transparent (default)		100 Mbps half duplex
10 Mbps full duplex	Transparent (default)		10 Mbps full duplex
10 Mbps half duplex	Transparent (default)		10 Mbps half duplex
100 Mbps half duplex	Transparent (default)		Auto negotiation
10 Mbps half duplex	Transparent (default)		Auto negotiation
100 Mbps full duplex	Local	Local	Auto negotiation
10 Mbps full duplex	Local	Local	Auto negotiation
Integrated FO port with FX standard (100 Mbps full duplex)	–	Local	Auto negotiation
Integrated FO port with FL standard (10 Mbps full duplex)	–	Local	Auto negotiation
100 Mbps full duplex	Not permitted (Full and half duplex mode must not be combined)		100 Mbps half duplex
10 Mbps full duplex			10 Mbps half duplex
100 Mbps full duplex	Not permitted (Different transmission speeds)		10 Mbps full duplex
100 Mbps full duplex			10 Mbps half duplex
100 Mbps half duplex			10 Mbps full duplex
100 Mbps half duplex			10 Mbps half duplex

8 Supply voltage

The module is operated with a +24 V DC SELV.

8.1 Operation as an individual device

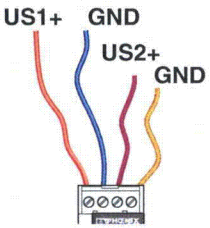


Figure 8 Connecting the power supply

- Provide the supply voltage for the module via terminal blocks US1 and GND.
- As an option, an additional power supply unit can be connected to terminal blocks US2 and GND to provide a redundant voltage supply.

8.2 Combined operation with system power supply unit

As an alternative, the devices can be supplied using the MINI-SYS-PS-100-240AC/24DC/1.5 system power supply unit (Order No. 2866983). This is connected via two ME 17,5 TBUS 1,5/ 5-ST-3,81 DIN rail connectors (Order No. 2709561).

- Usually the system power supply unit is mounted as the first device in a topology. A second power supply unit can be used to create a redundant supply concept.

9 Twisted pair interface (TP port)

9.1 10/100Base-T interface

The FL MC 10/100 BASE-T/FO G1300ST has an Ethernet interface on the front in RJ45 format, to which only twisted pair cables with an impedance of 100 Ω can be connected. The data transmission speed is 10/100 Mbps.

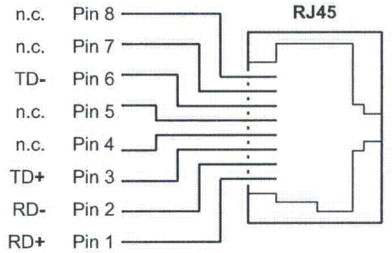


Figure 9 Pin assignment in RJ45 format

Connection

- Push the Ethernet cable with the crimped RJ45 connector into the interface until it engages with a click. Please observe the keying of the connector.

NOTE: Use shielded cables/connectors

Only use shielded twisted pair cables and corresponding shielded RJ45 connectors.

9.2 MDI/MDIx changeover

In general, line cables (1:1) are required between structure components and termination devices. Crossover cables, on the other hand, are used to connect two devices of the same type.
The integrated crossover switch on the FL MC 10/100 BASE-T/FO G1300ST makes cable selection easier, which means that the device can always be connected using line cables (1:1). For crossed cable assignment, simply set the switch to the "Cross" position.

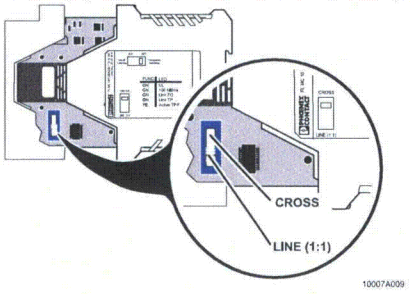
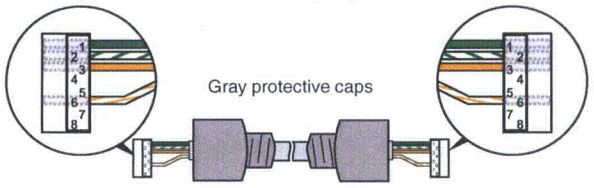


Figure 10 MDI/MDIx changeover

The correct switch position can be selected using the following table.

	PC/RFC	IBS gateway	I/O bus terminal	Switch	Hub	FO converter
PC/RFC	Cross	Cross	Cross	Line	Line	Line
IBS gateway	Cross	Cross	Cross	Line	Line	Line
I/O bus terminal module	Cross	Cross	Cross	Line	Line	Line
Switch	Line	Line	Line	Cross	Cross	Cross
Hub	Line	Line	Line	Cross	Cross	Cross
FO converter	Line	Line	Line	Cross	Cross	Cross

Pin assignment of line cable (1:1)



(1)	Green	(1)
(2)	Green/white	(2)
(3)	Orange	(3)
(6)	Orange/white	(6)

Figure 11 Line connection

10 Diagnostic indicators

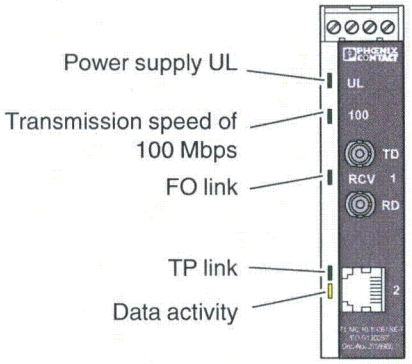


Figure 12 Diagnostic indicators

Power supply UL

The green "UL" LED lights up when the module is supplied with power.

Transmission speed of 100 Mbps

The green diagnostic LED lights up when both interfaces are operating at a transmission speed of 100 Mbps.

When one or both interfaces transmits data at 10 Mbps, the LED goes out.

FO link (link control fiber optic path (FO))

The line monitoring function checks the connected cable segment for an interrupt. The partner must transmit link or data signals.

The green LED lights up if no error has occurred. An interface that is not being used or a termination device that is switched off is indicated as an error and the LED goes out.

TP link (link control TP path (RJ45))

The line monitoring function checks the connected cable segment for a short circuit or an interrupt. The partner must transmit link or data signals.

The green LED lights up if no error has occurred. An interface that is not being used or a termination device that is switched off is indicated as an error and the LED goes out.

Data activity

The yellow "Activity" LED flashes according to the amount of data that is being transmitted or received by the TP/FO interfaces.

The LED remains permanently lit when only one auto negotiation signal is present at the FO converter and the second connection is not connected.
Faulty cables or device failures can thus be detected easily.

11 Fiber optic interface (FO port)

Connection notes

WARNING: Damage to eyes

During operation, do not look directly into transmitter diodes, or use visual aids to look into the glass fibers.

The infrared light is not visible.

NOTE: Do not remove dust protection caps too soon

Dust protection caps should only be removed just before the connectors are connected. They prevent contamination of the transmit and receive elements.

The same applies for the protective caps on the connectors.

NOTE: Install fiber optics correctly

Observe the cable manufacturer's technical data when handling the various fiber optic cables.

In order for the communication path to be protected against interference, the permissible values for the bending radii, tensile force, and pressure force must not be exceeded.

11.1 Fiber optic (FO) connection

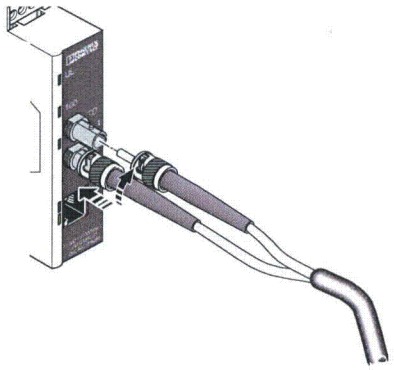


Figure 13 Connecting the B-FOC (ST®) connector

1. Connect the fiber optic cable to the B-FOC (ST®) connector for the transmit and receive channel and push the connector clamp mechanism downwards.
2. Secure the connection with a quarter turn to the right.

Connecting two FO converters

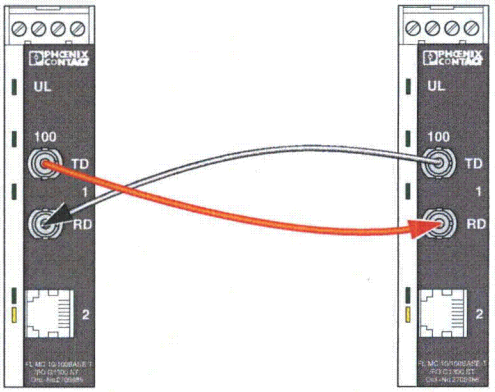


Figure 14 Signal direction for the fiber connection

NOTE: Connecting two FO converters

When connecting two FO converters, note the signal direction of the fiber optics.

Module 1 fiber connection "TD" (transmitter) to module 2 fiber connection "RD" (receiver).

11.2 Optical power measurement after initial installation

After the installation of a fiber optic link, the optical power can be checked before the receiving device using a fiber optic measuring device.

The transmitting device must be operated at an ambient temperature of 20°C ... 30°C. Temperature-related fluctuations are already taken into account in the limit values.

Measuring the optical power

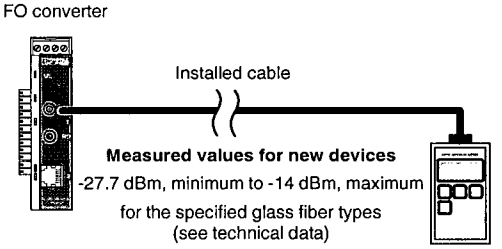


Figure 15 Measuring the optical power

The dBm values indicated already take into account the 3 dB system reserve, temperature influences, and aging of the transmitter/receiver.

This system reserve must be maintained in each fiber optic system to reduce physical aging of the optical transmitter.

The values are valid for new devices. In the first year, aging may amount to 1 dB and to 0.2 dB in subsequent years.

- For glass fibers, set the measuring device to 1300 nm and the power measuring range to dBm.
- Remove the RJ45 connector to interrupt the data communication.
- Apply the operating voltage at the module (the green UL indicator lights up).
- The converter now transmits LINK pulses via the FO interface.
- Take measurements for the forward and return line. The specified measured values must be attained.

12 Configuration notes

Full duplex mode

In full duplex mode, the ranges specified in the technical data of the fiber optic interface apply.

Half duplex mode

In half duplex mode (10 Mbps), configuration must take into account the expansion rules for collision domains. This can lead to considerable reductions in the range.

In order to reach maximum transmission distances and maximum transmission performance, the connected devices must be set permanently to 100 Mbps and full duplex transmission.

The transmission mode (half/full duplex) can be optimized using the mode selector switch (see "Mode selector switch" on page 7).

12.1 Expansion of collision domains

In order to determine the limits of the system configuration, a study must be performed. The result of the study must be positive, otherwise transmission errors may occur. We recommend compiling a plan of the network and proceeding systematically to find and study all possible signal paths and collision domains.

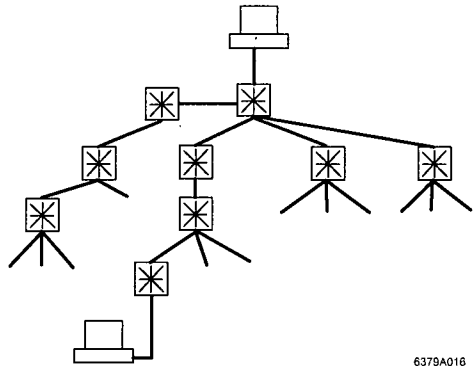


Figure 16 Network plan

12.2 Considering the PEV (Path Equivalent Value)

The PEV describes the signal delay of an Ethernet packet as a result of a network component. It is specified in meters. For reliable data transmission, the sum of all the signal delays including the total length of the installed cables must not exceed 4520 m between any two network devices within a collision domain.

The study must include network cards (NIC), hubs, FO converters, and copper and fiber optic cables in the calculation.

Example	2 x network cards	at 140 m	280 m
	2 x hubs	at 420 m	840 m
	2 x FO converters	at 146 m	292 m
	1 x FO cable	at 1000 m	1000 m
	2 x TP cables	at 100 m	200 m
			Total 2612 m

Maximum length permitted (4520 m) - total (2612 m) =
Reserve for system expansion (1908 m)

12.3 Considering the PVV (Path Variability Value)

The PVV describes the sum of all the signal runtime fluctuations of an Ethernet packet through the network components of a signal path. It is specified in bit times (BT). For reliable data transmission, a maximum delay time of 40 BT is permitted between any two network devices within a collision domain.

The study must only include hubs, FO converters, and transceivers in the calculation.

Example	2 x network cards (already taken into account)	at 0 BT	0 BT
	2 x hubs	at 2 BT	4 BT
	2 x FO converters	at 1 BT	2 BT
	1 x FO cable (does not cause runtime fluctuation)	at 0 BT	0 BT
	2 x TP cables (do not cause runtime fluctuation)	at 0 BT	0 BT
			Total 6 BT

Maximum permitted bit time (40 BT) - total (6 BT) =
Reserve for system expansion (34 BT)

If both studies are positive, the system has been correctly configured.

Overview of PEV and PVV values for Factory Line products from Phoenix Contact

Component	PEV [m]	PVV [BT]
Network cards (NIC)	140	0
Hub/hub agent	420	2
Switch	140	0
FO converter (TP <-> FO)	146	1
Twisted pair cable/FO cable	1 per m	0