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UNITED STATES
NUCLEAR REGULATORY COMMISSION
WASHINGTON, D.C. 20555-0001

December 22, 1999

MEMORANDUM FOR: Stuart A. Richards, Director
Project Directorate IV and Decommissioning
Division of Licensing Project Management
Office of Nuclear Reactor Regulation

FROM: Steven D. Bloom, Project Manager, Section 2
Project Directorate IV and Decommissioning
Division of Licensing Project Management
Office of Nuclear Reactor Regulation

SUBJECT: SUMMARY OF MEETING HELD ON OCTOBER 28, 1999 WITH WESTINGHOUSE OWNERS GROUP TO DISCUSS ASIC-BASED REPLACEMENT MODULE (ABRM) DEVELOPMENT PROGRAM

On October 28, 1999, a public meeting was held at the U. S. Nuclear Regulatory Commission (NRC) offices in Rockville, Maryland, between industry respresentatives of Westinghouse, Southern Nuclear, and the NRC staff. The NRC requested this meeting to obtain some design and background information on the ASIC-Based Replacement Module (ABRM) Development Program. Attachment 1 is a list of attendees and Attachment 2 are the meeting handouts.

Mike Eidson from Southern Nuclear opened the meeting by providing the utilities' perspective on the ABRM progrm. Mr. Eidson is the Chairman of the ASIC Subgroup, which consists of eight utilities who sponsor the ABRM program. Following Mr. Eidson, Carl Vitalbo from Westinghouse provided a presentation on the ABRM program objectives, background, ASIC chip design features, and main board and personality module design. Mr. Vitalbo also provided the status of the test programs and the licensing approach.

During the presentation, Eric Lee, the NRC reviewer, raised concerns on the sufficiency of validation test vectors for the ASIC chip. He and Keith Mortenson, a NRC staff member, pointed out to Mr. Vitalbo that although Westinghouse performed about one quarter of million credible tests on ASIC, there are more than one million test vectors per each of the quarter million tests that Westinghouse performed. Mr. Vitalbo agreed with the staff, but stated that the ASIC design is simple and the amount of tests it performed is significant. In response, Mr. Lee asked how many transistors are in the ASIC chip. Mr. Vitalbo stated there are about 80,000 transistors in the ASIC chip, but the test vectors covers over 95 percent of them.

The presentation was concluded with Mr. Eidson's remarks, which included a request that the NRC continuously support the ABRM program, and cooperate in reviewing the ABRM topical report. Mr. Eidson noted that the ABRM program addresses obsolescence, spare part, and cost issues with existing analog equipment.

After the presentation, Mr. Lee met with Dick Miller from Westinghouse and raised some questions related to how the ASIC chip was designed and developed by Westinghouse's contractor Oak Ridge National Lab. Specifically, he raised the following questions:

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Who designed and developed the ASIC?

What are the qualifications of the designer?

Was there a design review?

Is there a design review specification?

What standard is used for manufacturing the ASIC chip (ATC)?

Project No. 694

Attachments: 1. Attendance List
2. Handouts

cc w/atts: See next page

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cc:
Mr. H. A. Sepp, Manager
Regulatory and Licensing Engineering
Westinghouse Electric Corporation
P.O. Box 355
Pittsburgh, PA 15230-0355

Mr. Andrew Drake, Project Manager
Westinghouse Owners Group
Westinghouse Electric Corporation
Mail Stop ECE 5-16
P.O. Box 355
Pittsburgh, PA 15230-0355

Mr. Jack Bastin, Director
Regulatory Affairs
Westinghouse Electric Corporation
11921 Rockville Pike
Suite 107
Rockville, MD 20852

MEETING WITH WESTINGHOUSE OWNERS GROUP

ATTENDANCE LIST

October 28, 1999

WESTINGHOUSE

D. Miller
C. Vitalbo

SOUTHERN NUCLEAR

M. Eidson

NRC

S. Bloom
E. Lee
F. Gallardo
H. Li
K. Mortensen
S. Mazumda
A. Marinos
J. Calvo
M. Eidson
D. Miller
C. Vitalbo

Attachment 1

7300A ASIC-BASED REPLACEMENT MODULE (ABRM) DEVELOPMENT PROGRAM

NRC MEETING

October 28, 1999

NRC White Flint Offices
Rockville, MD

Attachment 2

ABRM PROGRAM: AGENDA

- Program Objectives
- Background
- ASIC Chip Design
- Main Board & Personality Module Designs
- Validation Test Program
- Qualification Test Program
  - Environmental
  - Seismic
  - EMC
  - Fault
- Licensing
- Demonstration Project
- Utility Perspective

ABRM PROGRAM: OBJECTIVES

- The objective of this program is to utilize Application Specific Integrated Circuit (ASIC) technology to develop functionally equivalent replacement modules for the Westinghouse analog Process Protection System supplied as part of the original Nuclear Steam Supply System design.

ABRM PROGRAM: BACKGROUND

- October '95: WOG approved funding to develop ASIC-Based replacement modules for 7300, 7100 and Foxboro I&C platforms.

- February '98: Subgroup formed to continue development of the 7300 I&C platform.

- Subgroup Members:
  - Duquesne Light
  - Virginia Power
  - Wolf Creek
  - South Texas Project
  - South Carolina Electric & Gas
  - Southern Nuclear
  - ComEd
  - Northeast Utilities
  - Callaway

- Bi-Weekly conference calls held to discuss program status.

- 2-3 Meetings held each year with Subgroup and NRC.

ABRM PROGRAM: ASIC CHIP DESIGN

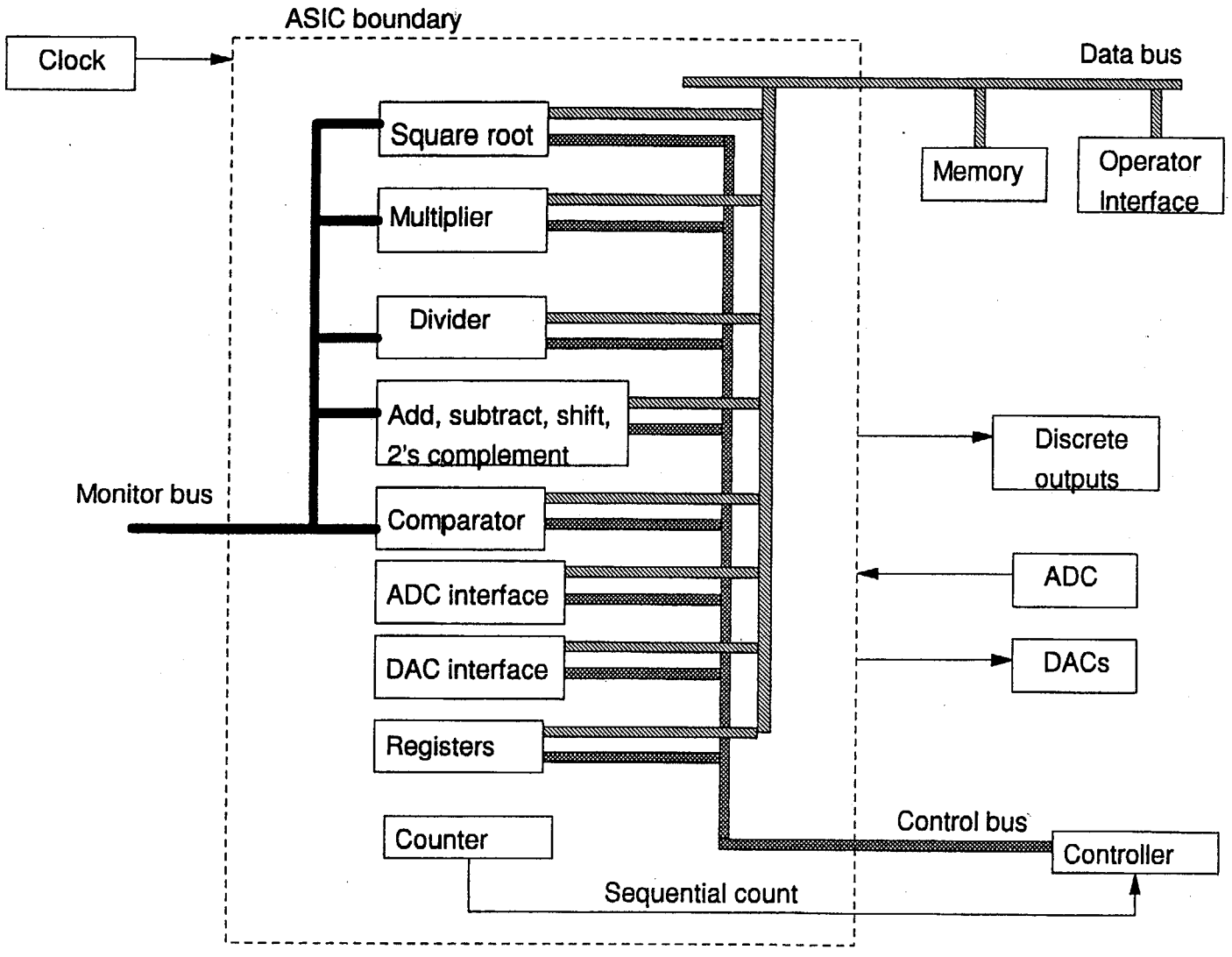
ORNL

- Designed ASIC chip as part of CRADA program with EPRI
- Fabricated ASIC prototype chips using ORBIT
- Designed Functional & Fault Test Vector Set
- In excess of 200,000 test vectors demonstrate functionality and testability of the design

ATC

- Tested ASIC design
- Tested Prototype ASIC chips manufactured by ORBIT
- Manufactured qualification & production ASIC chips
- Tested qualification & production ASIC chips using Functional & Fault Test Vector Set

ASIC and support components functional block diagram



DAC: Digital-to-analog converter
ADC: Analog-to-digital converter

ABRM PROGRAM: ASIC CHIP DESIGN

Vector Verification

- Integration testing revealed problems with multiplier & divider circuits in ASIC chip.

- Root cause analysis identified 2 reasons for error:
  1. Functional test vectors insufficient to detect error during initial design simulation testing
  2. Expected results from fault test vectors not verified by independent methods.

- Corrective actions implemented
  - Avoid over-carry situation
  - Enhanced functional & fault test vectors

- ORNL completed Functional test vector verification 2/98.

ABRM PROGRAM: ASIC CHIP DESIGN

Fault Grading

Eight individual hardwired sections of ASIC tested:

Section	Fault Coverage
• ADC	94.7%
• Adder/Subtractor	99.2%
• Multiplier/Divider	96.4%
• Square Root	96.6%
• Comparator	98.7%
• DAC	94.4%
• Registers	99.4%
• Controller/Counter	Counts to 64K

- Total number of Test Vectors: 26,950

ABRM PROGRAM: ASIC CHIP DESIGN

Vector Verification Summary

- Enhanced test vectors reduce probability of latent design or manufacturing defect becoming a common mode failure.
- Establishes the fact that, at time of test, the ASIC chip performs as intended, and that a failure in the future can be treated as a single random occurrence.
- This problem validated the premise that ASIC chip failures are detectable.
- This problem demonstrated thoroughness of test program.

ABRM PROGRAM: MB & PM DESIGN

Program Goals Have Been Met & Demonstrated:

- Addresses obsolescence issues associated with analog cards
- Direct card-for-card replacement for equivalent 7300 Analog Card
- Meet or exceed equivalent 7300 Analog Card performance
- Power consumption less than equivalent 7300 Analog Card
- Heat dissipation less than equivalent 7300 Analog Card
- Reliability equal to or greater than equivalent 7300 Card
- Cards are easier to calibrate and align
- Provides viable alternative to full-scale digital upgrade

ABRM PROGRAM: MB & PM DESIGN

Goals (continued)

- 1 Main Board and 14 Personality Modules can replace any one of 54 different 7300 analog modules.
- Design optimized to reduce board cost.
- Minimize impact on plant procedures
- Designed for higher operating temperatures
- Reduce spare parts inventory
- Standard Operator Interface makes it easier to learn & use
- Process functions are performed digitally (more accurate)

ABRM PROGRAM: MB & PM DESIGN

1. NAC: ANALOG COMPARATOR
2. NAL: ANALOG COMPARATOR
3. NCB: CONTROLLER
4. NCD: CONTROLLER DRIVER
5. NCH: FUNCTION GENERATOR
6. NLL: LEAD/LAG
7. NLP: LOOP P/S & ISOLATOR
8. NMA: MIXING AMPLIFIER
9. NMD: MULTIPLIER/DIVIDER
10. NRA: RTD AMPLIFIER
11. NSA: SUMMING AMPLIFIER
12. NSC: SIGNAL CONVERTER
13. NTD: TRACKING DRIVER
14. NVP: VOLTAGE-TO-PULSE CONVERTER

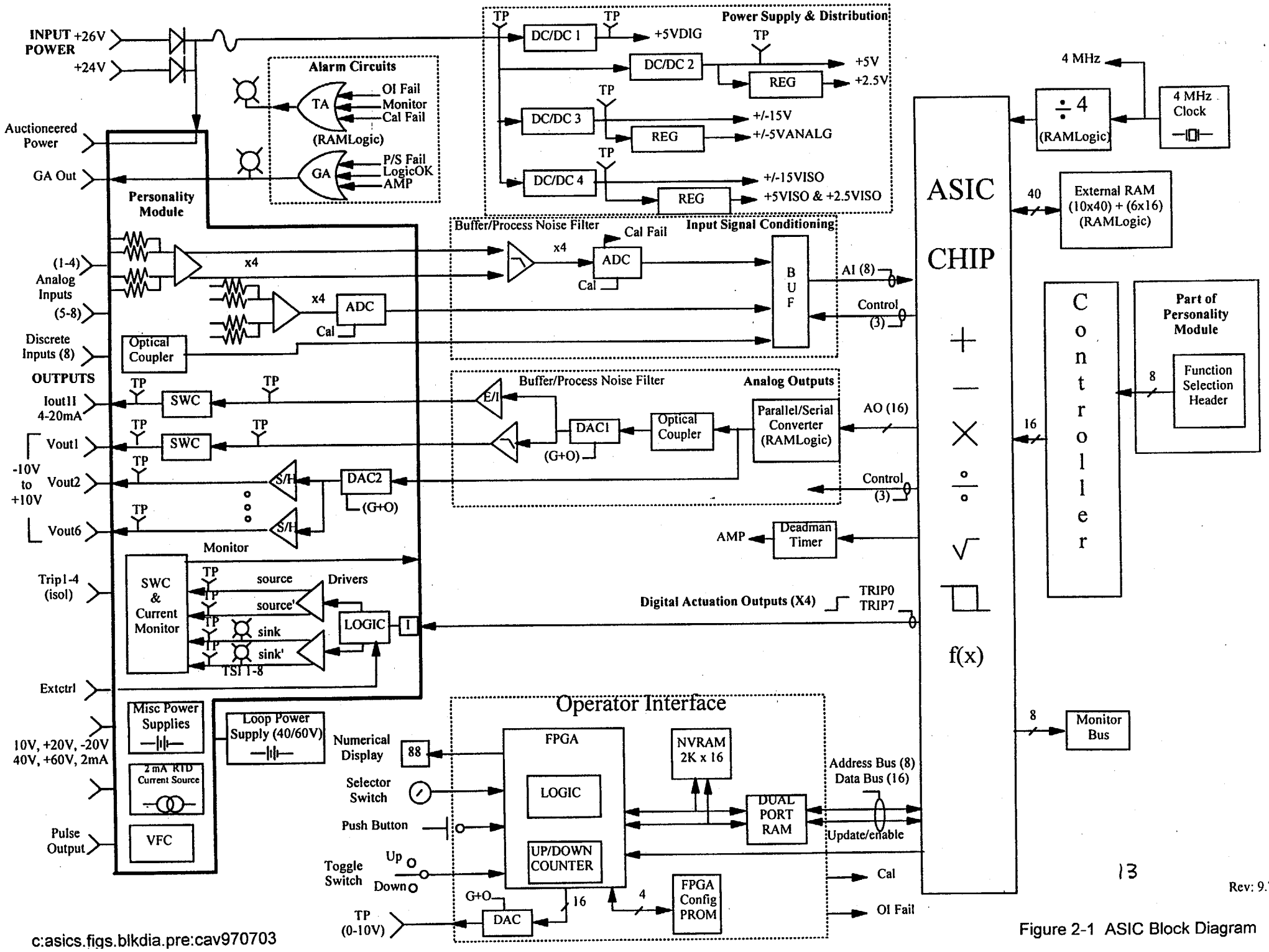


Figure 2-1 ASIC Block Diagram

ASIC CONTROLLER

(1)	Comparator Function	(NAC)
(2)	Comparator Function	(NAL)
(3-6)	Controller	(NCB)
(7)	Controller Driver	(NCD)
(8)	8 Segment Function Generator	(NCH)
(9-11)	Lead/Lag, Rate/Lag, Lag	(NLL)
(12-13)	Loop Power Supply	(NLP)
(14)	Mixing Amplifier	(NMA)
(15-16)	Multiplier/Divider	(NMD)
(17-19)	RTD Amplifier	(NRA)
(20-23)	Summing Amplifier	(NSA)
(24)	Signal Converter	(NSC)
(25)	Tracking Driver	(NTD)
(26-28)	Voltage-to-Pulse Converter	(NVP)
(64)	Test Segment	

Figure 2-3 ASIC CONTROLLER

ABRM PROGRAM: MB & PM DESIGN

SUMMARY OF FMEA RESULTS

- Calculated MTBF for all 14 MB/PMs > calculated MTBF for equivalent 7300 analog
- Calculated MTBF for all 14 MB/PMs >100,000 Hours
- All failure modes that affect board function are detectable by surveillance testing (same as 7300 Analog)
- Channel measurements verify that the module is functioning properly and detects the presence of process noise (same as 7300 analog)
- Some failures are immediately detectable via General Alarm (power supply, ASIC, clock, logic)

ABRM PROGRAM: MB & PM DESIGN

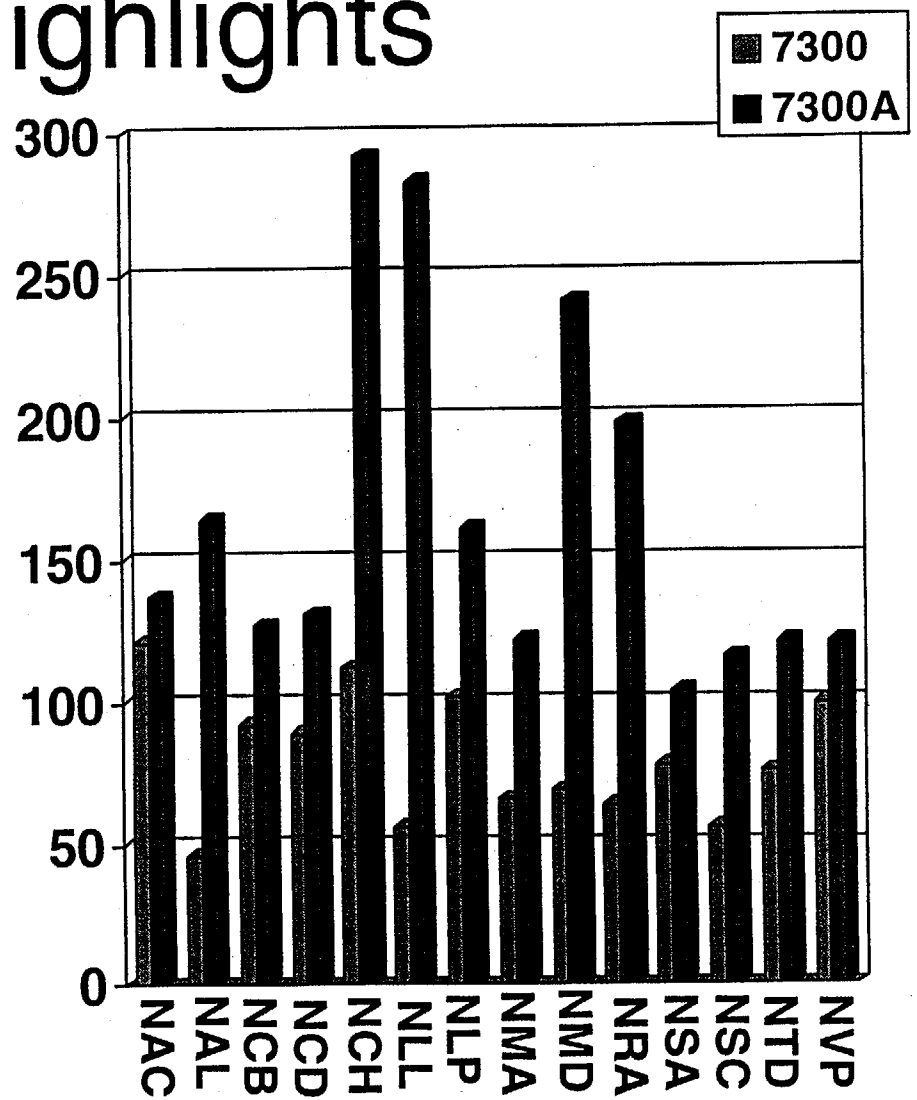
SUMMARY OF FMEA RESULTS (continued)

- Other failures are detectable via Periodic Surveillance Program (same as 7300 analog)
- All failures result in outputs High, Low, Drift, or As-Is (same as 7300 analog)
- No new failure modes

ABRM PROGRAM: MB & PM DESIGN

MTBF Highlights

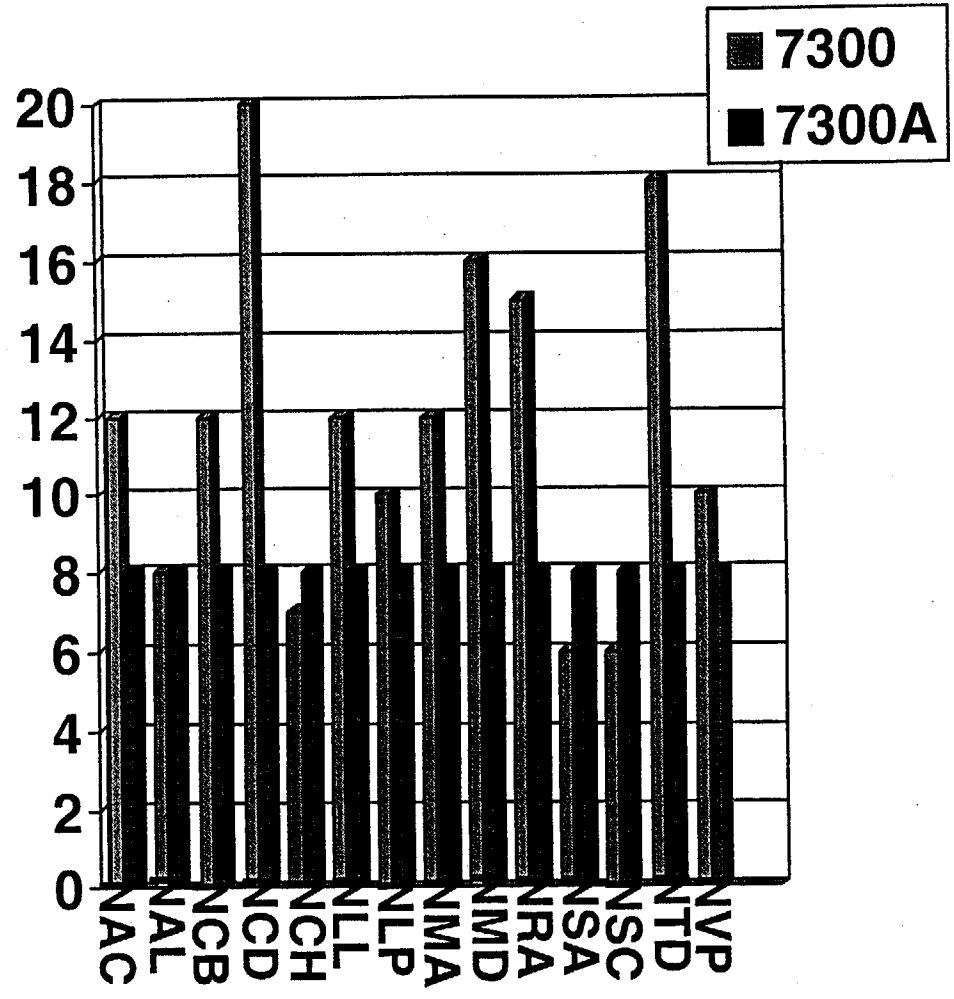
- 54/54 > 7300
- 54/54 > 100K Hrs.
- NSC (116K Hrs.)
- NMA (122K Hrs.)
- NCH (292K Hrs.)
- NLL (283K Hrs.)



ABRM PROGRAM: MB & PM DESIGN

Power Consumption

- 11/14 <= 7300
- 7.2W < 7300A < 8W
- NSC ~ 6W
- NCD ~ 20W
- NTD ~ 18W
- ASIC ~ 720mW
- Display ~ 250mW
- DC/DC ~ 80%



ABRM PROGRAM: VALIDATION TEST PROGRAM

- Formal testing of individual modules:
  - NXX Main Board
  - All 14 PMs
  - All 28 Controller algorithms
- Demonstrates that the ABRM:
  - Meets the performance requirements of the equivalent analog module it replaces.
  - Sequence of operations defined in the Controller algorithm correctly implements the desired process function.

ABRM PROGRAM: VALIDATION TEST PROGRAM

- Consists of three categories of stand alone tests:

  - Functional requirements tests
    (includes Operator Interface tests)

  - Abnormal Conditions & Events (ACEs) tests
    ("what happens if....." type tests)

  - Functional performance tests at abnormal temperature & humidity conditions

ABRM PROGRAM: VALIDATION TEST PROGRAM

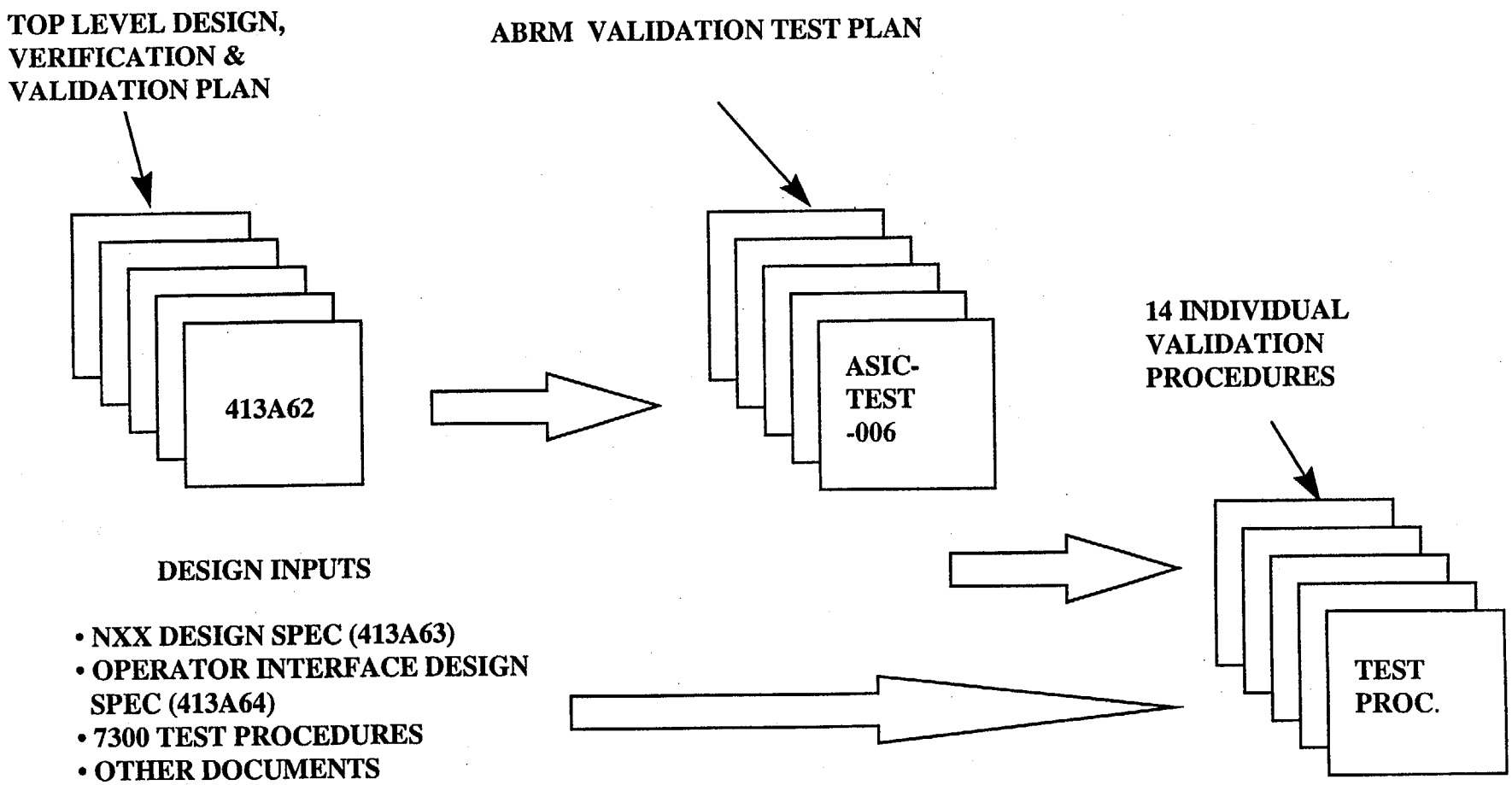
- The following specific types of tests demonstrate the suitability of the ABRM to function as a direct replacement for the analog modules:
  1. Time response tests
  2. Analog output signal accuracy tests at both normal & abnormal temperature & humidity conditions & at DC power supply voltage extremes.
  3. For NAL & NAC ABRMs, trip point accuracy tests at both normal & abnormal temperature & humidity conditions & at DC power supply voltage extremes.
  4. Dynamic response performance tests for ABRMs which perform time dependent functions.

ABRM PROGRAM: VALIDATION TEST PROGRAM

5. Overload and recovery tests to establish ABRM output signal response to an input signal overrange condition.
6. Analog output signal noise tests to establish acceptability of output signal noise levels.
7. Power dissipation & inrush current tests to establish full load power dissipation & inrush levels.
8. Module interaction tests to demonstrate any adverse affects caused by installing an ABRM adjacent to an analog 7300 modules.

ABRM PROGRAM: VALIDATION TEST PROGRAM

Procedure Generation Process



ABRM PROGRAM: VALIDATION TEST PROGRAM

Results to Date:

- Six of 14 modules have completed ambient testing:
  - NCH Function Generator
  - NLL Lead/Lag
  - NAC Analog Comparator
  - NAL Analog Comparator
  - NLP Loop Power Supply
  - NSC Signal Converter
- Includes functional verification per Design Spec & IB
- 4 of the 6 modules have completed environmental test at extremes of temperature & humidity (158 Degrees F & 95% RH)

ABRM PROGRAM: QUALIFICATION PROGRAM

General Test Selection Criteria:

- Test at least one of each module type
- Set up DTTA protection channel
  - Total of 16 modules
- Test other modules individually, NVP, NCB, NTD, NCD, NAC, NMA, NRA
- Results in testing 30 modules
  - Environmental (Temp/humidity)
  - Seismic
  - EMC

ABRM PROGRAM: ENVIRONMENTAL QUAL

Test Criteria

- Temperature & Humidity testing in accordance with WCAP-8587 Methodology.
- 158 Degrees F (70 Degrees C) which is 18 Degrees F (10 Degrees C) above analog design.
- 95% Relative Humidity.
- Supply voltage variations.

ABRM PROGRAM: ENVIRONMENTAL QUAL

Acceptance Criteria

- Maintain channel accuracy deviation to a maximum of 0.5% of span per 50 Degree F change.
- 0.1% of span for module test.

Test Configuration

- 30 ABRM Modules in 7300 DCF
- 16 ABRMs arranged as Delta_T/T_avg Protection Loop
- 6 ABRMs arranged in 3 Control loops
- 8 ABRMs arranged as stand alone modules

ABRM PROGRAM: ENVIRONMENTAL QUAL

Results

- Testing completed 6/99.
- ABRM modules passed with few anomalies.
- Anomalies appear to be hardware, operator error, or test set-up related.
- Investigative testing in progress.

ABRM PROGRAM: SEISMIC QUALIFICATION

Test Criteria

- Test in accordance with IEEE Standard 344-1987
  - Triaxial Shake Table
  - Multi-Frequency
  - Random Motion

- Seismic test levels:
  - 30 spectral g's peak acceleration
  - Approximately 5 g's ZPA (Zero Period Acceleration)
  - Frequency Spectrum: 1 Hz to 100 Hz.

ABRM PROGRAM: SEISMIC QUALIFICATION

Acceptance Criteria

- Maintain ability to perform safety function during and after SSE, zero residual effects.
- Contact outputs shall not chatter 2 milliseconds or greater.
- No change of state.

ABRM PROGRAM: SEISMIC QUALIFICATION

Test Configuration

- 30 ABRM Modules in 7300 DCF
- 16 ABRMs arranged as Delta_T/T_avg Protection loop
- 6 ABRMs arranged in 3 Control loops
- 8 ABRMs arranged as stand alone modules
- DCF mounted on Seismic Table

Results

- Testing completed 1/99
- 5 OBE and 2 SSE test runs completed
- All ABRMs meet functional and performance requirements before, during and after seismic test

ABRM PROGRAM: EMC QUALIFICATION

Test Criteria

- Perform testing in accordance with EPRI TR-102323, Revision 1

- Compare ABRM performance to equivalent analog module performance

ABRM PROGRAM: EMC QUALIFICATION

Acceptance Criteria

- Emissions (CE & RE)
  - Less than EPRI TR-102323 R1, Section 7

- Susceptibility (CS & RS)
  - No spurious trips (NAL, NAC)
  - < 25 mV deviation or equal to / greater than equivalent 7300 analog design.

- Surge & Electrical Fast Transient:
  - Deviation allowed during transient
  - Must recover to normal operation and accuracy
  - No permanent degradation

- ESD: Deleted, not common-mode failure mechanism

ABRM PROGRAM: EMC QUALIFICATION

Test Configuration

- Individual NXX Revision 1 Main Boards and PMs.
- Analog Modules for comparison.
- CHAR Services and Washington Labs contracted to perform EMC testing.
- Used 7300 Series Power Supply and Double Card Frame wired to accommodate each specific card style.

ABRM PROGRAM: EMC QUALIFICATION

Results

- Testing completed 8/99.

- Emissions (CE & RE):
  - ABRM emissions are less than allowable limits per EPRI TR-102323 R1, Section 7.
  - One CE data point (553KHz) exceeded limits but with acceptable margin of 15-20 dB.

ABRM PROGRAM: EMC QUALIFICATION

Results (continued)

- Susceptibility (CS & RS):
  - Generally same as / better than equivalent 7300 analog design
  - Subsequent testing performed to demonstrate minimum 8 dB margin over measured plant data for each individual card.
  - 2 modules still outside 8 dB acceptance criteria (NLP & NRA)
  - Modules are being evaluated.
- Surge & Electrical Fast Transient:
  - All cards returned to initial conditions after test.
- ESD: Test deleted.

ABRM PROGRAM: FAULT QUALIFICATION

Test Criteria

- Fault testing performed in accordance with WCAP-8892A, "Westinghouse 7300 Series Process Control System Noise Tests."

- Fault voltages:
  - 125 and 250 Vdc, Differential & Common Mode.
  - 125 and 580 Vac, Differential & Common Mode.
  - Short circuit on output.

ABRM PROGRAM: FAULT QUALIFICATION

Acceptance Criteria

- Maintain capability to perform protection function.
- No solder splatter.
- Damage to card is permitted.

Test Configuration

- NXX/NLP Voltage-to-Voltage isolator
- NXX/NSC Voltage-to-Current isolator
- 24 tests total

Results

- Testing completed 10/99
- Isolator modules passed

ABRM PROGRAM: LICENSING

- There have been eight NRC meetings to date:
  1. 12/8/95
  2. 3/26/96
  3. 11/12/96
  4. 3/18/97
  5. 7/15/97
  6. 12/3/97
  7. 5/6/98
  8. 9/25/98
- There have been four Licensing submittals to date:
  1. 7/10/97: TOC, Introduction, System Description, Design Verification & Validation Plan
  2. 6/5/98: FMEA Summary
  3. 8/14/98: Documentation package consisting of specs, drawings, test procedures, etc.
  4. 8/9/99: Seismic Report WCAP-15215, Rev. 0
- Balance of submittals to be made as efforts are completed

ABRM PROGRAM: LICENSING

7300 ABRM LICENSING SUMMARY REPORT

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2.0 *System Design Description
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4.0 ASIC Chip Test Results
5.0 Validation Test Plan
6.0 Environmental, *Seismic, EMC & Fault Test Results
7.0 *Reliability Assessment & FMEA Results
8.0 WEC Safety Evaluation
9.0 Supplemental Report on Response Time Testing
10.0 Regulatory Criteria Compliance
11.0 References

ABRM PROGRAM: LICENSING

NRC Review Plan:

- NRC Audit.
- Review Design, Verification & Validation Process.
- Review responsibilities of WEC, ORNL & ATC.
- "Thread Path" reviews using Design, Verification & Validation Plan as road map.

ABRM PROGRAM: LICENSING

NRC Efforts to Date:

- Participated in periodic meetings and provided feedback.
- Reviewed documentation submittals.
- Visited the following facilities:
  - WEC NPBU (Pittsburgh) to review design process.
  - ORNL (Oak Ridge) to review ASIC design process.
  - Northrop Grumman ATC (Baltimore) to observe ASIC manufacturing process.

ABRM PROGRAM: LICENSING

- NRC expressed six concerns during development phase:
  1. Translation of 7300 design requirements into ABRM design.
  2. Testing & Testability of the ABRM Design.
  3. Conformance to Technical Specification accuracies.
  4. Implementation under 10CFR50.59.
  5. Test versus field conditions.
  6. Use of CAD/CAE software design tools.
- All concerns were addressed in 12/3/97 meeting with no outstanding issues.
- Design Verification & Validation Plan developed to meet licensing & Appendix B requirements.
- Extensive program documentation developed to meet QA requirements & for transfer to utilities.

ABRM PROGRAM: LICENSING

Licensing Schedule

• Chip Test Results	10/99
• Qualification Test Results	11/99
• Safety Evaluation & Reg. Compliance	11/99
• Validation Test Results	01/00
• Licensing Summary Report Submittal	02/00
• NRC SER	03/00
• Ship Hardware to Demo Plant	03/00

ABRM PROGRAM: DEMONSTRATION PROJECT

- STPNOC will demonstrate ABRM design
- ABRM cards will be installed in Boric Acid Tank Level and NR RCS Temperature Indication channels
- 4 ABRMs (plus spares) will be provided to STPNOC
  - 2 NXX/NLP
  - 1 NXX/NAL
  - 1 NXX/NRA
- Installation planned for Spring 2000

ABRM PROGRAM: DEMONSTRATION PROJECT

- WEC scope includes the following:
  - FAT Procedure generation for 5 ABRMs.
  - Technical Manual.
  - Support from Pittsburgh.

- STPNOC to issue Field Reports after 1 month & 12 months of operation.

ABRM PROGRAM: UTILITY PERSPECTIVE

- WOG Core Group Design Review: Conducted 8/96.
- WOG Subgroup Test Program: Conducted 2/99 - 4/99.
  - 12 of 14 applications tested by utility I&C technicians & engineers.
  - Instruction Manuals reviewed.
  - Modules tested using actual plant set-up procedures and application information.
  - Comments/findings addressed by ABRM Program engineers.
- Training Sessions
  - STP training session conducted 11/98.
  - Open training session scheduled for 12/99.
  - Additional training will be scheduled in 2000

ABRM PROGRAM: UTILITY PERSPECTIVE

- Westinghouse & Subgroup members are committed to ABRM Program.
- View program as viable means to extend the life of the Westinghouse 7300 Process Protection & Control System.
- Program addresses obsloescence, inventory/spare parts, and calibration reduction issues.
- Utility technician & engineer involvement in the design review & test programs provides additional assurance that ABRM Program products will satisfy future needs.
- Request continued NRC Staff support of the ABRM Program schedule.